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High Power High Efficiency Semipolar InGaN Light Emitting Devices for Solid State Lighting

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in

Materials

by

Daniel Louis Becerra

Committee in charge:

Professor Shuji Nakamura, Chair

Professor Steven P. DenBaars

Professor Claude Weisbuch

Professor Jon A. Schuller

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The dissertation of Daniel Louis Becerra is approved.

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Jon A. Schuller

_____

Claude Weisbuch

_____

Steven P. DenBaars

_____

Shuji Nakamura, Committee Chair

November 2016

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VITA OF DANIEL LOUIS BECERRA
December 2016

EDUCATION

Bachelor of Science in Materials Science and Engineering and Engineering and Public Policy, Carnegie Mellon University, May 2012 (college and university honors)

Doctor of Philosophy in Materials, University of California, Santa Barbara, December 2016

PROFESSIONAL EMPLOYMENT

2012-2016: Graduate Research Assistant, Department of Materials, University of California, Santa Barbara, Santa Barbara, CA

Summer 2011: Research Experience for Undergraduates Intern, Department of Materials Science and Engineering, Northwestern University, Evanston, IL

May 2010- January 2011: Research Intern, Aquion Energy, Inc., Pittsburgh, PA

2009-2012: Undergraduate Research Assistant, Department of Materials Science and Engineering, Carnegie Mellon University, Pittsburgh, PA

PUBLICATIONS

D.L. Becerra, D.A. Cohen, R.M. Farrell, S.P. DenBaars, and S. Nakamura. *Effects of active region design on gain and carrier injection and transport of CW (20-2-1) semipolar InGaN laser diodes*. Appl. Phys. Express **9**, 092104 (2016).

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K. Gelžinytė, R. Ivanov, S. Marcinkevičius, Y. Zhao, D.L. Becerra, S. Nakamura, S.P. DenBaars, and J.S. Speck. *High spatial uniformity of photoluminescence spectra in semipolar (20-21) plane InGaN/GaN quantum wells.* J. Appl. Phys. **117**, 023111 (2015).

CONFERENCE PRESENTATIONS (first author only)

D. L. Becerra, D.A. Cohen, R.M. Farrell, S.P. DenBaars, and S. Nakamura. *High Efficiency Semipolar III-Nitride Lasers for Solid State Lighting.* 25th International Semiconductor Laser Conference, Kobe, Japan, September 2016.

D. L. Becerra, D.A. Cohen, R.M. Farrell, S.P. DenBaars, and S. Nakamura. *The Effect of Quantum Well Number and Mg Compensation by Oxygen on the Performance of CW Semipolar III-Nitride Lasers.* 18th International Conference on Metal Organic Vapor Phase Epitaxy, San Diego, CA, July 2016.

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AWARDS

Outstanding Graduate Student Research Achievement Award, Solid State Lighting and Energy Electronics Center, University of California, Santa Barbara, 2016

Honorable Mention, Best Paper Award, 2016 International Semiconductor Laser Conference

Outstanding Graduate Student Research Achievement Award, Solid State Lighting and Energy Electronics Center, University of California, Santa Barbara, 2014

Eagle Scout, Boy Scouts of America, 2007

ABSTRACT

High Power High Efficiency Semipolar InGaN Light Emitting Devices for Solid State Lighting

by

Daniel Louis Becerra

The impact of solid state lighting on the world has been remarkable. The improvement in efficiency and lifetime, the reduced environmental impact and the new design space of solid state lighting when compared to traditional incandescent or compact fluorescent lighting is dramatic. Still, improvements can be made to improve and accelerate the adoption of this technology.

Light Emitting Diodes (LEDs), the basis of solid state lighting, are impacted by the problem of efficiency droop, whereby the efficiency of LEDs peaks at low current density and declines dramatically with increasing current. This limits the power out per chip and requires many chips to be used to create an incandescent equivalent replacement fixture. In this dissertation, several ways of addressing this problem and other efficiency limits of solid state lighting will be addressed.

Utilizing novel properties of alternative planes of the gallium nitride (GaN) crystal, LEDs can be fabricated with reduced droop. These semipolar planes differ from the c-plane (the plane all commercial devices are grown on) in that they have reduced polarization-related

effects, which increases the quantum efficiency. Semipolar LEDs with wider active regions to reduce carrier density and limit Auger recombination are demonstrated.

Laser Diodes (LDs) can also be used to improve the efficiency of solid state lighting. LDs have higher brightness than LEDs and are not impacted by efficiency droop above threshold, so it is possible to run LD chips at high currents and obtain orders of magnitude higher power per chip, with the potential to reduce size and thus cost of solid state lighting fixtures. Semipolar planes can again be used to overcome efficiency limits of c-plane LDs as well.

The design of LEDs and LDs are presented in this dissertation. Beginning with metalorganic chemical vapor deposition (MOCVD) growth, continuing through nanofabrication, packaging, and testing, all facets of semipolar nitride devices will be discussed. Simulations are used throughout to gain additional insight into experimental results and predict future behavior.

Semipolar LEDs with low droop and power of 1 W from a small 0.1 mm^2 chip and continuous wave (CW) semipolar LDs with 11 % wall plug efficiency are demonstrated. The internal loss and injection efficiency of semipolar LDs is reported for the first time. An accurate absorption model is used to predict gain and transparency current density. Reduced threshold current and improved differential efficiency LDs with fewer quantum wells in the active region are demonstrated. Many considerations to improve the wall-plug efficiency of LDs are discussed, and a path to world record wall plug efficiency is described at the conclusion.

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1. Introduction

A. Solid State Lighting

Solid state lighting is the culmination of decades of advances in light generating technologies. Old technologies such as candles or incandescent light bulbs use radiation given off by heating a material to generate light, losing vast amounts of energy to heat. Fluorescent lamps use around one quarter of the energy of an incandescent, but they contain toxic mercury. In contrast, solid state lighting based on light emitting diodes (LEDs) converts electricity directly to light, realizing ten times or more improvement in efficiency from incandescent and about three times as efficient as compact fluorescents with no toxic materials. The U S Department of Energy estimates solid state lighting by 2035 will penetrate into over 90% of the lighting market, and reduce energy use by over 75%.[1] This technology and other energy efficient technologies are essential for combating climate change and sustainably growing the world economy. It is always important to continue to drive up efficiency and drive down cost, and this dissertation will discuss improved efficiency LEDS as well as using laser diodes (LDs) instead of LEDs for the next generation of solid state lighting. An introduction to the technologies will first be given.

1. LED Basics

The visible light emitting diode (LED) was first reported by Holonyak in 1962.[2] The simplest LED consists of a semiconductor p-n junction where electrons and holes will recombine to emit light of a particular bandgap corresponding to the bandgap of the material.

The first LED demonstrated by Holonyak emitted light at 710 nm. The reader is directed to Schubert's book *Light Emitting Diodes* for more reading on the subject of early LEDs.[3] LEDs of short wavelengths were then demonstrated up to the green spectral range, but the blue LED remained elusive for many years. Shuji Nakamura finally succeeded in fabricating the first blue LED by using InGaN in 1991.[4] Many amazing developments in InGaN LEDs quickly followed. The use of a p-i-n structure with quantum wells (QWs) as the active region to further confine carriers led to greatly improved performance, and to the eventual demonstration of InGaN laser diodes by Dr. Nakamura.[5] However, LEDs still suffer from certain challenges to high efficiency high current density operation, including the efficiency droop phenomenon, which will be discussed in the next sections.

The combination of the blue LED with a yellow emitting phosphor yttrium aluminum garnet doped with cerium gave the first white LED lights. This combination is quite efficient, with efficiencies demonstrated about 250 lm/W, but the color quality can be poor. Utilizing multiple LEDs and or phosphors can improve the quality of the light, usually at the cost of lower efficiency.[6]

2. Laser Basics

The laser diode (LD) is a semiconductor device that emits coherent light via stimulated emission. Its design is similar to that of an LED, i.e. p-i-n structure, but careful attention must be paid to confine photons as well as carriers to get gain in the laser cavity. The reader is directed to later sections of the dissertation and to an excellent introduction to the laser presented in *Diode Lasers and Photonic Integrated Circuits* by Coldren, Corzine and Mašanović for a more detailed explanation of laser operation.[7] Lasers can also be used for

solid state lighting. They have the benefits of increased efficiency at high current density and a lower form factor than LEDs that can realize lower cost, as can be seen in Figure 1-1.[8]

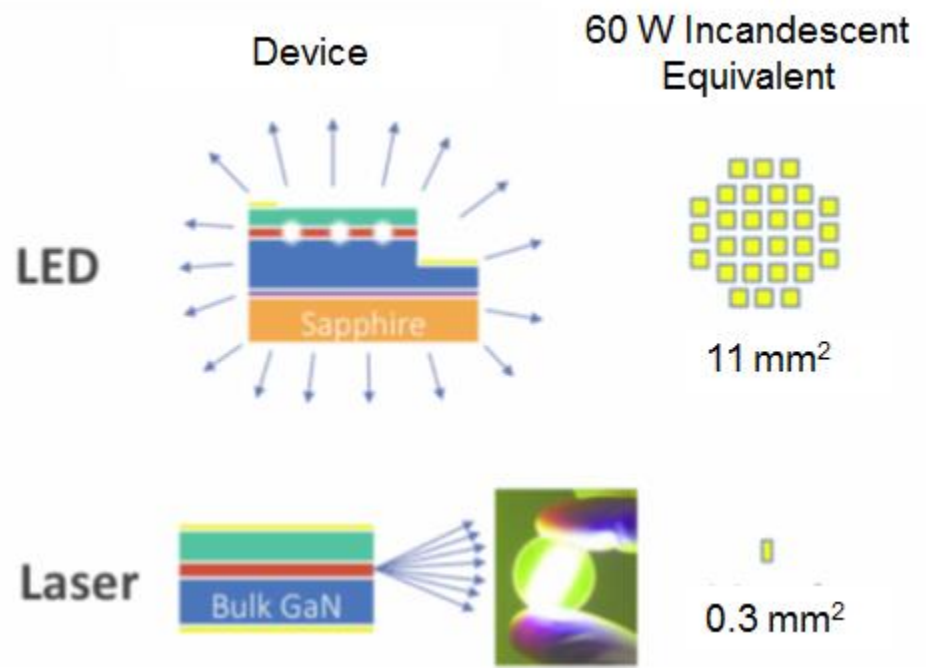

Figure 1-1: LD Device Footprint Reduction

Additional applications for LDs in lighting include automotive headlights, stage and stadium lighting, and other high intensity directional lighting.

B. Gallium Nitride

The semiconductor gallium nitride (GaN) and its alloys with Aluminum (AlGaN) and Indium (InGaN) are the basis of all light emitting devices discussed in this dissertation. These materials can emit light across the visible spectrum by tuning the composition of the ternary InGaN alloy by wavelength as shown in Figure 1-2. This simple figure ignores polarization and strain effects, discussed later.

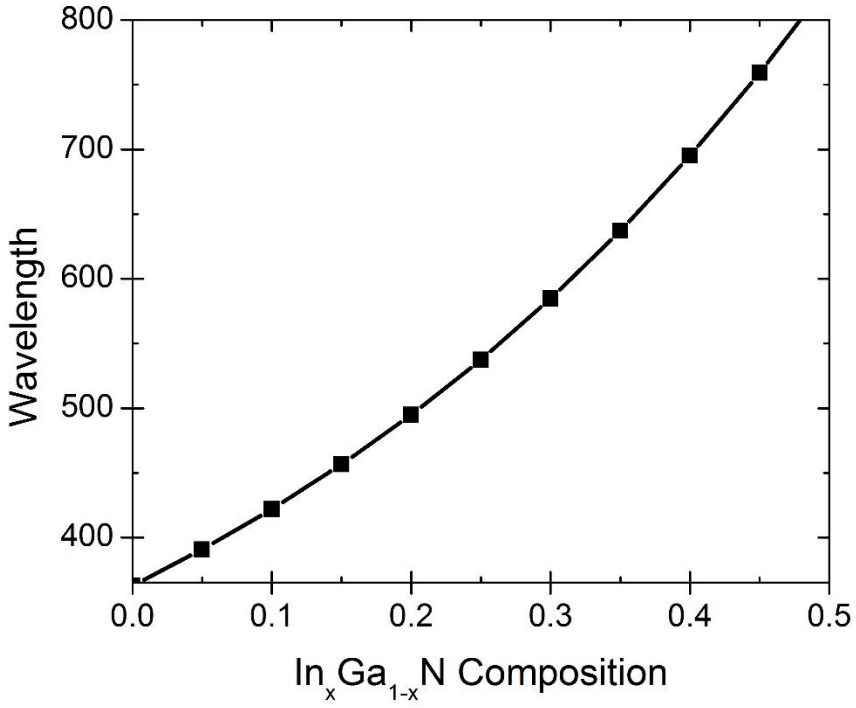

Figure 1-2 InGaN Alloys Emission Wavelength vs In Composition [2]

1. GaN Basics

Due to the low symmetry of GaN wurtzite crystal structure (Figure 1-4), spontaneous polarization fields will exist along the *c* basal plane.[9] Additionally because of this lack of symmetry, piezoelectric polarization exists in strained layers of InGaN or AlGaN due to the lattice mismatch between these layers and GaN.[10], [11] These fields will produce detrimental effects including the separation of electron and hole wavefunctions leading to reduced radiative recombination, and the quantum confined stark effect (QCSE) and coulomb screening effect which will shift emission wavelength with increasing current. The magnitude of the total polarization fields, both spontaneous and piezoelectric, is shown with respect to the angle from the c-axis and indium composition in Figure 1-3.[12] It should be mentioned that these

polarization fields can be exploited to produce beneficial effects (such as 2-dimensional electron gases) for power electronic devices.

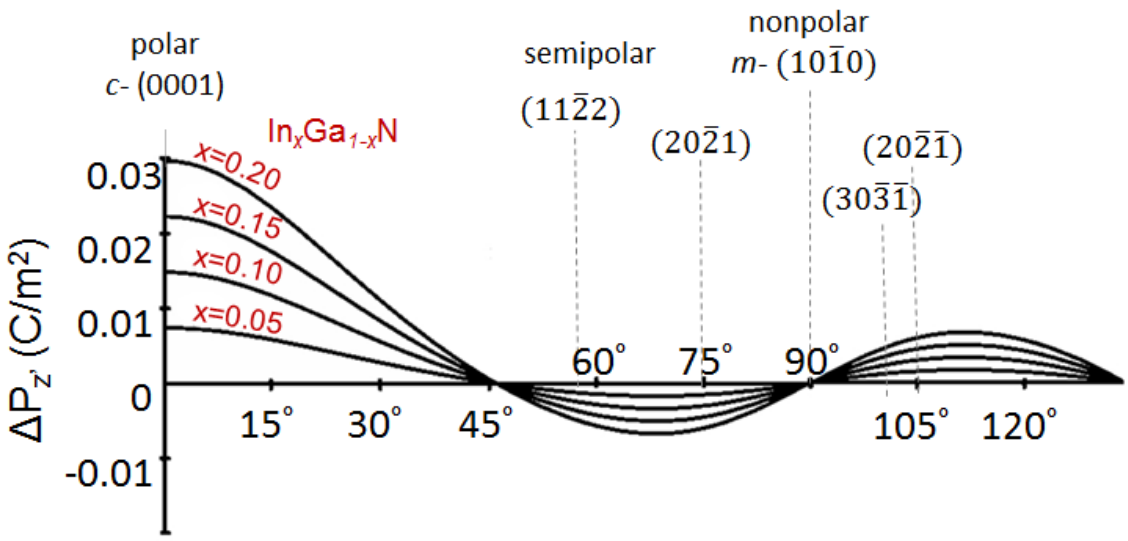

Figure 1-3: Polarization vs Angle in GaN[12]

2. Semipolar GaN

Other orientations of GaN can be used other than the c-plane to mitigate the effects of polarization. Since the polarization depends on the angle, selecting a plane which is at some angle from the c-plane will reduce the magnitude of the polarization fields and thus increase wavefunction overlap and mitigate detrimental effects of polarization. These planes are termed nonpolar (m, a) for planes with no polarization due to being perpendicular to the c-axis, and semipolar for planes at some angle in between. Certain semipolar planes, including (20$\bar{2}$1), with inclination angles less than 90° have polarization fields which will redshift the emission wavelength, leading to longer wavelength emission at lower indium compositions, which shows promise for green devices. [13] Other semipolar planes with inclination angles greater

than 90° have the added benefit of the polarization of the crystal opposing the built in electric field of the p-n junction, leading to further enhanced wavefunction overlap.[14] Those planes include semipolar $(20\bar{2}\bar{1})$ and $(30\bar{3}\bar{1})$. Devices grown on these two planes form the bulk of the dissertation. Figure 1-4 shows various semipolar planes.

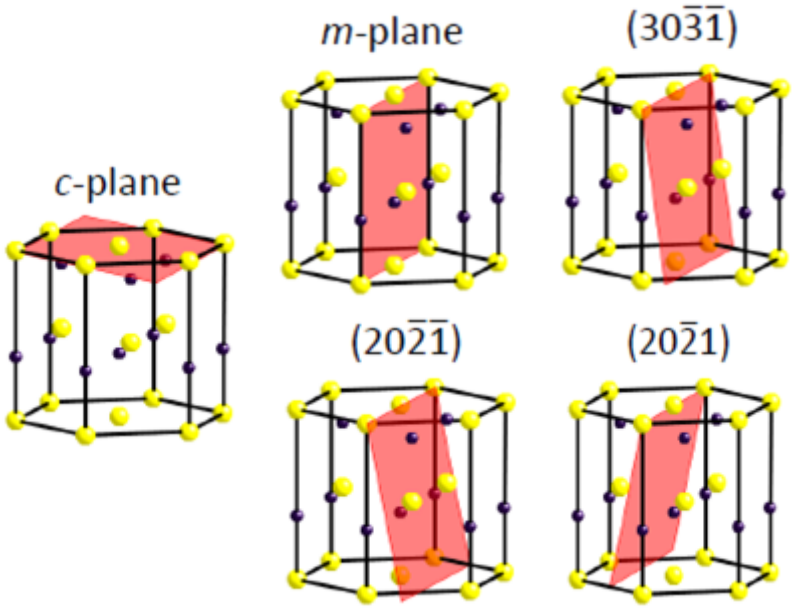

Figure 1-4: GaN Crystal Planes

Figure 1-5 shows the calculated band diagrams for a single quantum well device comparing c plane and the semipolar $(20\bar{2}\bar{1})$ and plane at a high current density of 3 kA/cm^2.

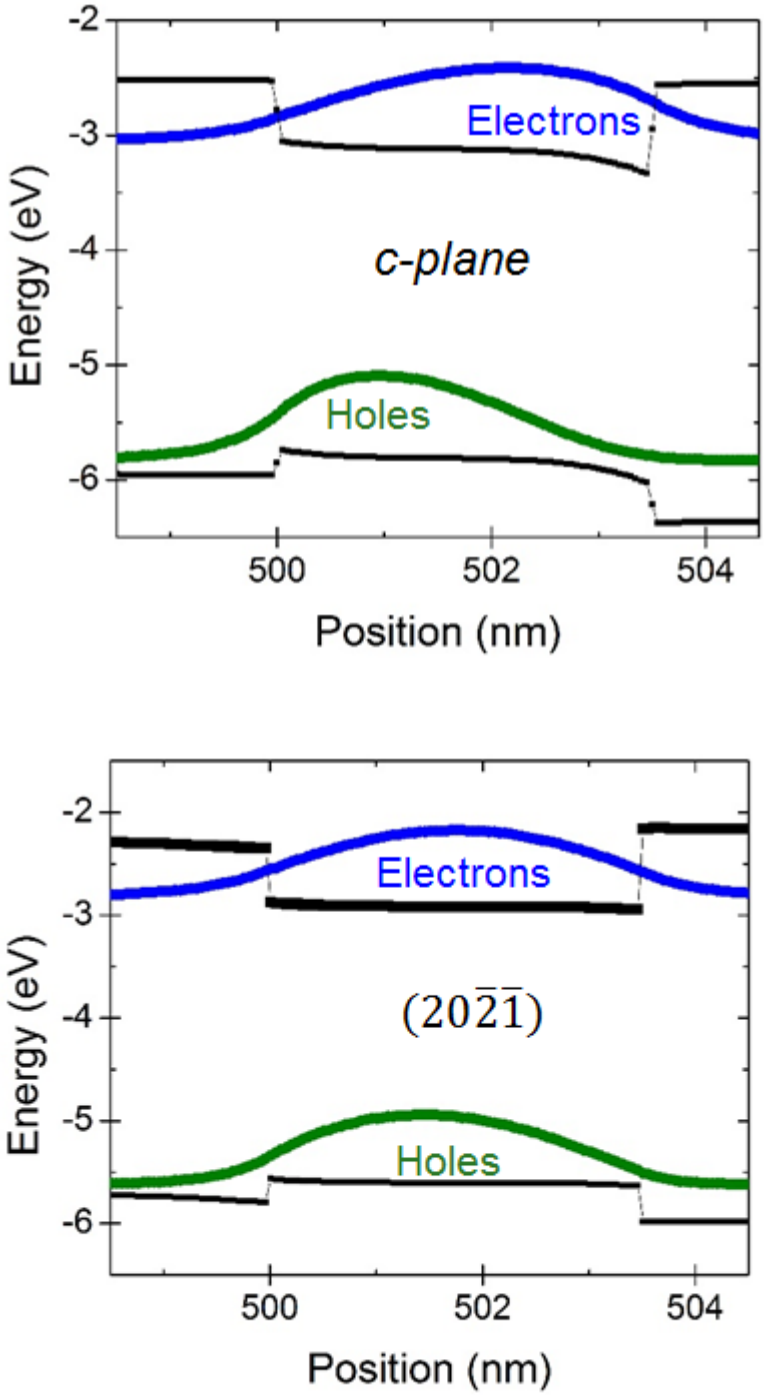

Figure 1-5: Band diagrams comparing 20-2-1 and c-plane Higher wavefunction overlap: ~0.95 on (20$\bar{2}\bar{1}$), ~0.7 on (0001) at ~3 kA/cm2

The higher wavefunction overlap can be clearly seen.

C. LED Details

InGaN LEDs grown on semipolar planes have demonstrated emission from violet to green, much like on the polar c-plane.[15]–[17] LEDs consists of an (usually) undoped active region made up of InGaN [usually one or more quantum wells (QWs)], with p- and n-GaN regions on either side. Usually a highly doped electron blocking layer (EBL) is placed between the active region and the p-side to prevent electron leakage and improve hole injection. In order to understand how the devices perform and how to improve them, terms and performance metrics must first be defined.

3. Metrics

The most basic metric is the wall plug efficiency (WPE). This is the ratio of injected current that produces light output. This can be split into two efficiencies: an electrical or voltage efficiency and an external quantum efficiency (EQE). The voltage efficiency refers to how efficiency voltage applied to the device supplies carriers to the device. The EQE is the ratio of photons produced to the number of carriers supplied to the device. The EQE can then be separated into a light extraction efficiency (LEE) and an internal quantum efficiency (IQE). The IQE refers to how efficiently electrons and holes recombine to emit light of the desired wavelength, and the LEE refers to how efficiently photons of that wavelength escape from the device and are emitted into air. EQE can be measured simply from a Light Output Power-Current curve (L-I), whereas LEE must be modeled and IQE can then be measured indirectly. The IQE can also be measured using low temperature photoluminescence (PL) or with more difficult experimental techniques.[18], [19]

4. LED droop

The EQE of the LED is the metric most frequently reported (WPE is second most, and it will almost always follow the trend in EQE with increasing current). For InGaN LEDs, highest reported EQEs are above 80 %.[20], [21] However, there is a well discussed phenomenon whereby the EQE of an InGaN LED peaks at low currents and declines rapidly with increasing current. This is termed efficiency droop and has been the subject of much research.[22]–[31] The cause of droop is often debated. Evidence exists supporting Auger recombination (where an electron and hole recombine and give their energy to a third carrier rather than produce a photon) as a large contributor. [22], [23] Carrier leakage is also identified as a possible cause.[25], [26] In either case, reducing the carrier density by enlarging the active region should reduce both of these effects. This is difficult to do on c-plane because of the large separation in wavefunctions that will occur in wide quantum wells. Using semipolar planes with reduced polarization fields, wider quantum wells can be grown without much wavefunction separation. So, on semipolar planes one can make efficient LEDs with significantly lower droop, and this will be addressed in more detail in Chapter 3. [16], [32]

D. LD Details

LDs are similar to LEDs in growth and fabrication with several key differences. Lasers must confine photons as well as electrons and holes. These photons must be confined in a resonant cavity with feedback from mirrors at either end. Then as carriers are injected into the active region and recombine, the population of photons reaches a point where the emission of a photon causes another photon to be emitted in the same phase (stimulated emission), leading to gain and lasing. Thus there are usually layers of lower refractive index InGaN, GaN, or AlGaN on either side of the high refractive index QWs of the active region to provide that

confinement. The active region of serval quantum wells will typically be surrounded by a separate confining heterostructure (SCH) for this purpose.[33]

5. Terms and Performance Metrics of LDs

Some amount of optical loss (or absorption) will be present in any cavity. In order for a laser to reach threshold, the point at which lasing begins, the gain must exceed the loss. First, the cavity is absorbing. As more carriers are added and more light emitted, gain will begin to overcome the loss. The point of net zero gain is the transparency condition. The point at which gain is greater than loss is the threshold condition.

Much like LEDs, the WPE is wall plug efficiency is the ratio of injected current that produces light output. This can be split into three efficiencies for lasers: threshold efficiency, voltage efficiency, and differential efficiency. The threshold efficiency, η_{th}, is how far above threshold the laser can be operated. This is maximized with low threshold current and high current operation. The voltage efficiency, η_v, is the photon energy over the operating voltage. This is maximized by keeping the operating voltage of the device low. The differential efficiency, η_d, is how efficiently carriers are converted to emitted photons in the active region above threshold. This is maximized be keeping the internal loss as low as possible, and keeping injection efficiency high. Injection efficiency, η_i , is a measure of the number of carriers that contribute to stimulated emission in the active region as a portion of all carriers provided to the device (similar to IQE for LEDs). Equation 1-1 shows the expression for WPE expressed in terms of the other three efficiency terms.

$$WPE = \eta_{th}\eta_v\eta_d = \frac{I - I_{th}}{I} * \frac{h\nu/q}{V} * \eta_i \frac{\alpha_m}{\langle\alpha_i\rangle + \alpha_m} \quad (1\text{-}1)$$

The differential efficiency is expressed as an injection efficiency times a mirror loss over a total loss. The mirror loss is useful loss, the photons exiting the cavity as laser light. The internal loss, α_i , is the parasitic loss related to absorption by dopants, free carriers, etc. The injection efficiency is a measure of how carriers supplied to the device reach the active region and recombine. The mirror loss can be calculated according to Equation 1-2:

$$\alpha_m = \frac{1}{L}\ln(\frac{1}{R}) \quad (1\text{-}2)$$

6. Laser Design Basics

The structure of an InGaN LD is similar to that of an LED, with a quantum well active region and p- and n-GaN regions on either side. The LD also needs layers designed to confine photons as well. This consists of layers with lower refractive index than the quantum well active region. In many c-plane lasers p- and n-AlGaN is used as the cladding layer.[5], [34] This requires thick or high composition layers of AlGaN to provide refractive index contrast. There are challenges to growing these kind of layers related to lattice mismatch stress/strain and electrical properties of AlGaN, in particular p-AlGaN. In contrast one could also use low composition InGaN as a waveguiding layer in a separate confining heterostructure configuration and remove AlGaN cladding layers. This is termed an AlGaN-cladding-free design and has been demonstrated by our group many times on various planes of GaN.[35]–[38]

7. State of the Art Diode Lasers: GaAs, InGaN

GaAs LDs emitting in the red spectral range have had the benefit of decades of research and are presently the most efficient semiconductor lasers. WPE over 70% has been demonstrated.[39] The threshold, voltage and differential efficiencies of these lasers are all about 90 %. The injection efficiencies are 95 % or higher and the internal loss about 1 cm^{-1} or lower.

InGaN LD efficiencies remain lower. To the author's knowledge, the highest WPE InGaN LDs are from Nichia Corp. at about 40%.[40] Figure 1-6 shows a breakdown of the losses due to each of the three parts of the WPE equation for this LD. Figure 1-7 shows the same breakdown for high efficiency GaAs lasers from nLight Corp.[39]

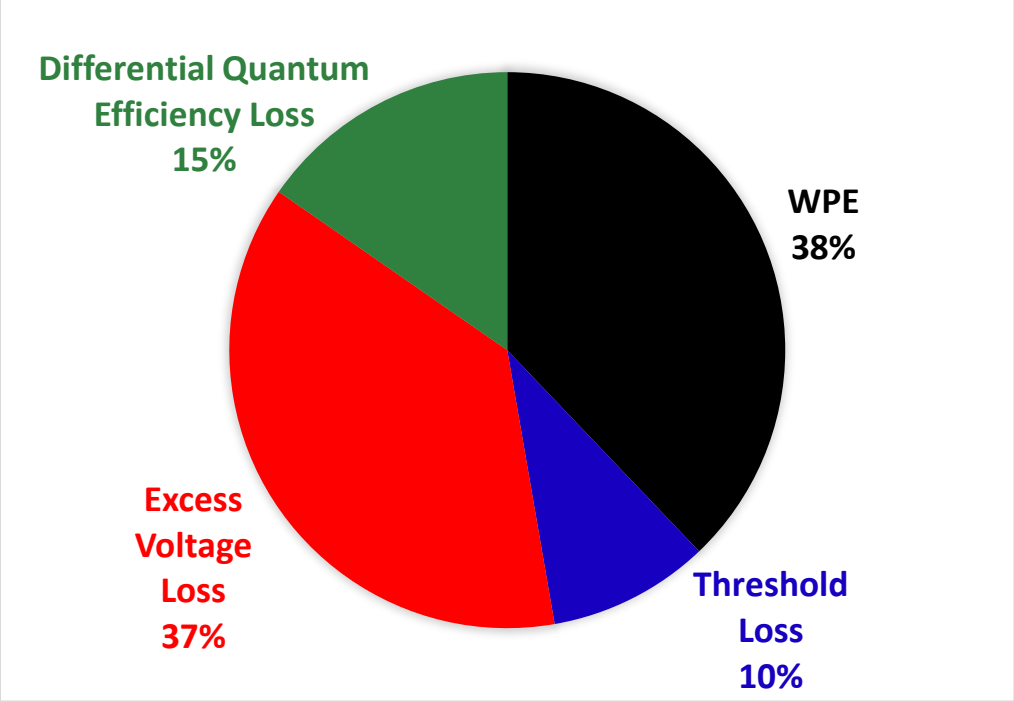

Figure 1-6: State of the Art GaN WPE Breakdown: InGaN 450 nm Lasers, Nichia 2013, c-plane

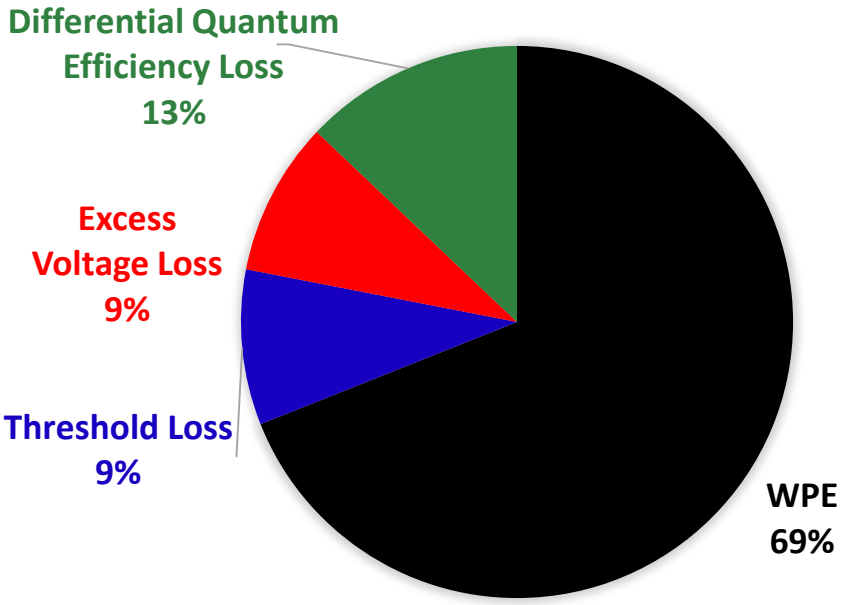

Figure 1-7: InGaAs WPE Breakdown 980 nm InGaAs LD from nLight

The threshold efficiency is similar to GaAs state of the art, but voltage and slope efficiencies remain lower. This laser diode was grown on the c-plane.

8. Semipolar LD advantages

The reduction of polarization fields from moving to semipolar or nonpolar devices should improve threshold efficiency, and possibly also voltage and differential efficiency. Both the improved wavefunction overlap and changed density of states will contribute to more efficient lasing. On semipolar planes, the valence band degeneracy is broken leading to reduction of hole effective mass and the inversion of more efficient carriers, which should also reduce the transparent carrier density. [41] Additionally, the improved wavefunction overlap will yield higher gain per carrier above transparency, thus the differential gain will be higher. The radiative lifetime is reduced on semipolar planes, from 6 to 9 ns on c-plane to 2 to 3 ns on

semipolar planes. This has been experimentally verified by Melo et. al. [41] Prior semipolar LD results at UCSB have shown WPE of a few percent, improvement will be shown throughout this dissertation.

E. Summary and Synopsis of the Dissertation

Solid state lighting has revolutionized the way we get light, and advances in this field are rapid. The goal of the dissertation was to improve the efficiency of light emitting devices based on GaN, with the goal of improving solid state lighting. The basics of LED and LD operation were introduced in this chapter, and the top line efficiency metrics for each device were introduced. Chapter 2 will discuss the growth of semipolar (Al, Ga, In)N in detail. Chapter 3 will discuss improvement in LED droop by increasing the active region thickness, and Chapter 4 will introduce LD design and discuss considerations for high power and long wavelength emission, and present a case study of a coupled laser design. Chapter 5 discusses detailed improvements to laser fabrication by improving contacts, heatsinking, facets and the development of a topside n-contact processes. Chapter 6, 7, and 8 discuss laser device results in detail. Chapter 6 focuses on the measurement of internal loss and injection efficiency, Chapter 7 discusses improvements by reducing the number of quantum wells in the active region, and Chapter 8 discusses oxygen compensation. Chapter 9 will summarize the work and present future work.

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2. Overview of Semipolar MOCVD Growth

Growth on the conventional c-plane of GaN has been well studied. This dissertation will discuss growth on nonpolar and semipolar planes of GaN, and discuss c-plane growth only as it compares to growth on relevant planes for this dissertation. All growth for this dissertation was done using UCSB Nippon Sanso MOCVD reactor #6.

A. Substrate Selection

The first GaN devices were grown on sapphire substrates. The lattice mismatch necessitated the development of buffer layer technology to control misfit and threading dislocations in the films. [1] Other substrates for heteroepitaxy are possible, but much work must be done for each substrate individually to optimize the growth and control defects. In contrast the growth on freestanding bulk GaN can be free of these interface defects, leading to high quality devices. Additionally, homoepitaxy is essential for easy access to various planes of GaN. Semipolar substrates can be created by precisely cutting a bulk GaN boule at the correct angle to expose the desired growth plane. The substrate is then polished and cleaned before growth. All semipolar devices discussed in this work used freestanding GaN semipolar substrates from Mitsubishi Chemical Corporation (MCC).

B. Nonpolar Growth: Developments and Continuing Issues

UCSB demonstrated some of the first m-plane LEDs and LDs in the mid-2000s.[2], [3] These devices were promising but significant growth problems existed. Some were addressed by template optimization and moving to miscut substrates. [4] This proved to be very successful for devices emitting in the 390-420 nm violet spectral range. However, issues remained with growth of LEDs and LDs at longer wavelengths[5], [6] which motivated the movement to semipolar planes.

C. Semipolar Template Growth

Growth on semipolar planes has its own distinct advantages and challenges. This dissertation will focus on growth on semipolar planes $(20\bar{2}1)$, $(30\bar{3}1)$, $(20\bar{2}\bar{1})$ and $(30\bar{3}\bar{1})$. Much early semipolar growth development was done by Hsu, Hardy, Zhao, Pan, and others.[7]–[12] These semipolar planes have certain polarization properties that have been discussed previously or will be discussed later. For growth on these planes, the conditions of the first epitaxial layer, the template, must first be optimized, and these optimized conditions will be discussed here. During template growth, it is important to maintain a smooth surface for the growth of subsequent layers. The conditions can be different depending on the plane. [13] Growing on bulk GaN substrates simplifies this process, but work must still be done to optimize the template.

The GaN substrates from MCC are polished using a proprietary series of mechanical and/or chemical polishing steps. It is suspected, but cannot be confirmed for proprietary reasons, that there is some weak surface or subsurface damage. Thus, an unoptimized template will propagate this damage in the form of defects such as those seen in Figure 2-1.

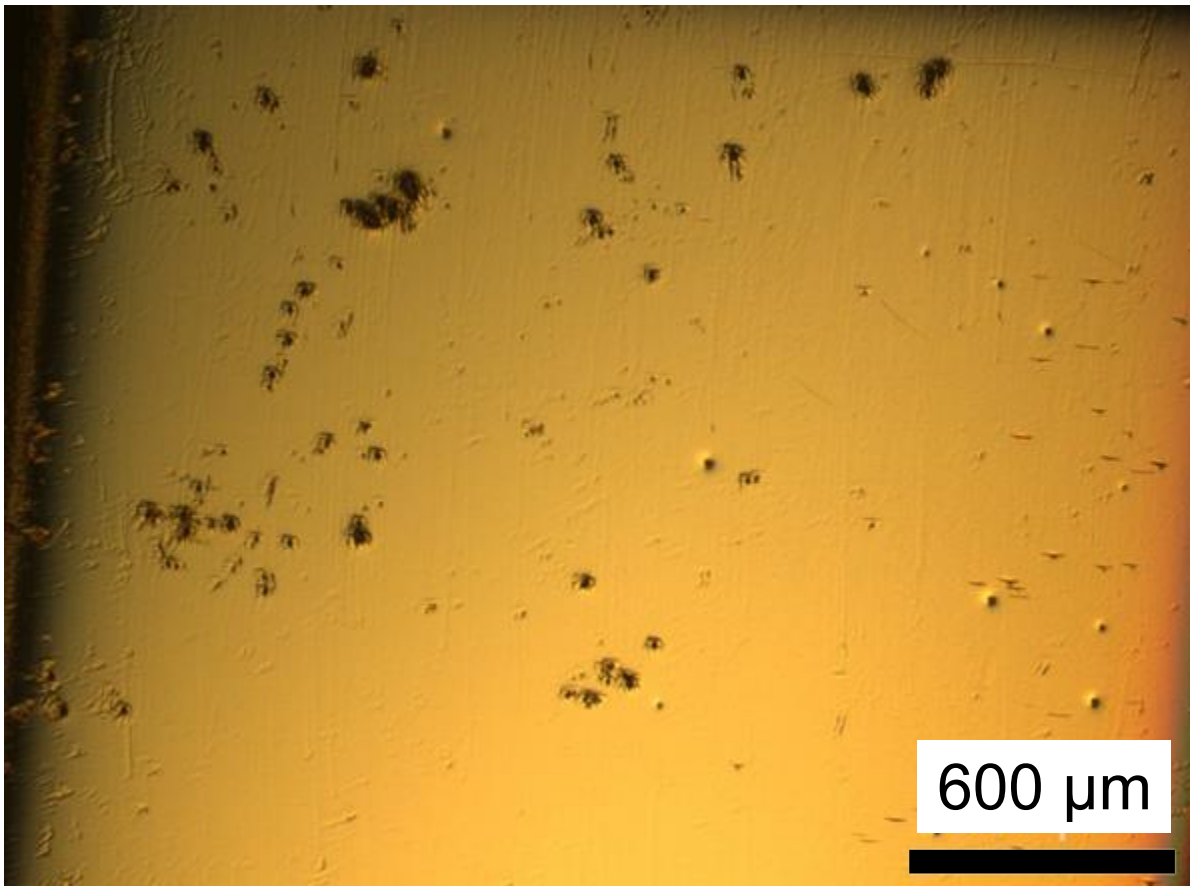

Figure 2-1: Surface of Device with Poor Template Condition

For the sake of completeness, the full template conditions will be described, however it is unclear which conditions make an impact since an exhaustive study was not done. The substrate is first heated in hydrogen carrier gas which will weakly etch and smooth out the substrate surface. The optimized template is grown at high temperatures between 1150 and 1200 C heater set temperature.[1] The template is generally n-doped, although this is not always the case, as will be described in subsequent sections. The n-type dopant used is disilane Si_2H_6. Then a GaN template is grown in nitrogen carrier gas using Trimethyl gallium (TMG). The

[1] All growth temperatures mentioned in this dissertation will be heater set point temperatures. The wafer temperature is approximately 50 - 100 C lower.

growth rate is approximately 4 μm/hr. The template thickness is approximately 1 μm. Template thickness was shown to have a negative impact; i. e. thicker templates produced more defects. Figure 2-2 shows a device with an optimized template.

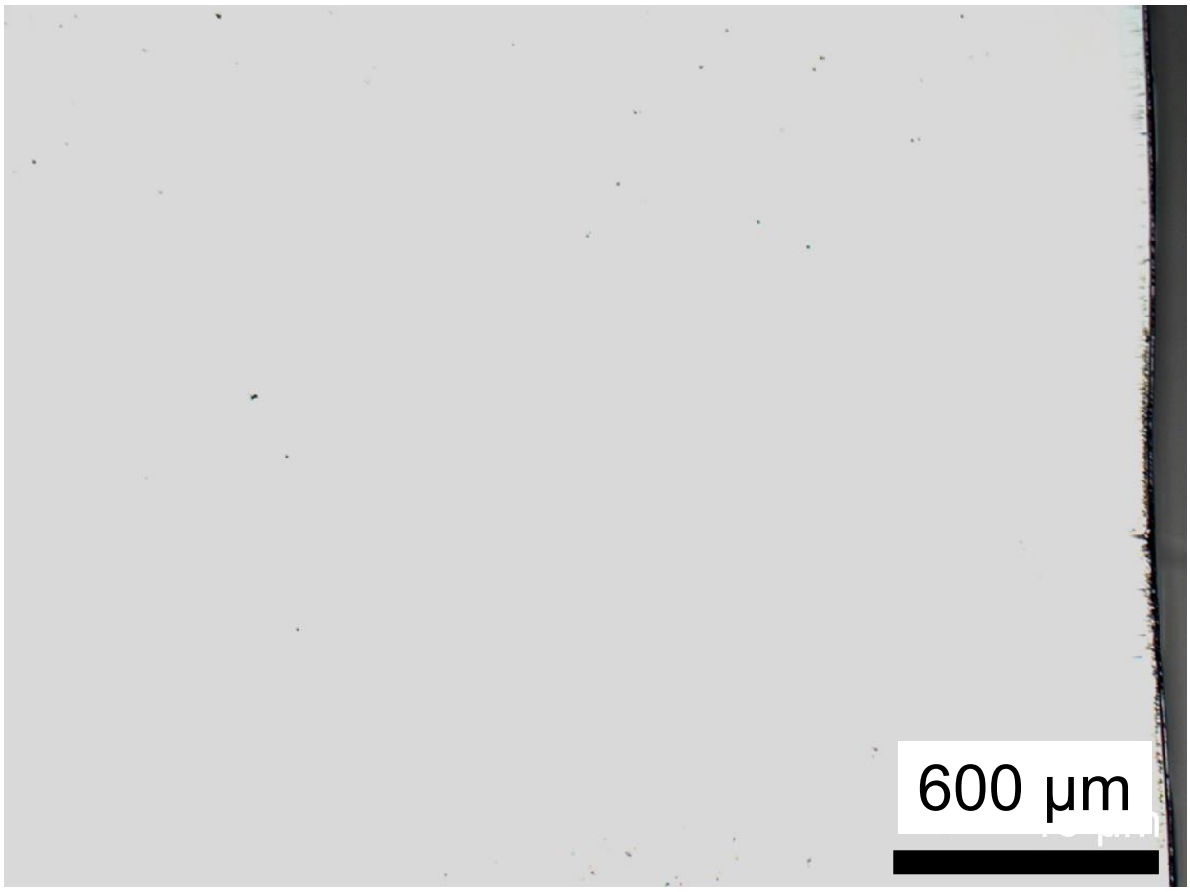

Figure 2-2: Surface of Device with Optimized Template

Other ways of optimizing this template condition may be possible. These defects are theorized to originate from individual-substrate specific polishing damage or miscuts, and then propagate through subsequent layers if the template condition is not optimized.

After the template, the source gas was changed to triethlyl gallium (TEG) and the temperature was ramped down to conditions for the next layer. Growth continued so as to not provide any growth pauses for impurities to be incorporated. The gas is switched to TEG for

the lower carbon incorporation it affords. The temperature is ramped downward for the growth of InGaN layers.

D. Semipolar Growth of InGaN Layers

The growth of InGaN is the subject of much research. Issues such as alloy fluctuations and carrier localization will not be discussed here, but the reader is pointed to many studies of this topic.[14]–[17] Several issues related to InGaN growth will be discussed. First, InGaN must be grown at lower temperatures than GaN or AlGaN because of the possibility of desorption, which introduces the potential for increased impurities or defects at lower growth temperatures. Additionally, the growth temperature controls the incorporation of indium as well as the trimethyl indium (TMI) flow, at lower temperatures more indium will incorporate, and at higher TMI flows more indium will incorporate. Unlike AlGaN, InGaN displays saturation behavior where the TMI flow vs In content curve will flatten at high In flows, so temperature is a more reliable input parameter. For, dopant incorporation, higher temperatures will generally incorporate less Mg and Si, the dopants used for p- and n-type respectively.

The device active layers in this dissertation will consist of InGaN layers of various compositions for emission in the range of violet to blue to green. These will be QWs of a few nm thick sandwiched between thicker GaN barriers of 5-10 nm. An important issue when growing ternary alloys on semipolar planes is the relaxation and formation of misfit dislocations at the alloy interface due to dislocation glide along available slip planes. According to extensive work by Romanov and colleagues, relaxation will occur at or slightly above the predicted Matthews-Blakeslee critical thickness for relaxation of resolved shear stress. [18] The glide occurs on the basal (0001) plane. [19], [20] Figure 2-3 shows calculated critical thickness for some relevant planes. Relaxation will occur at or within tens of

nanometers above this calculated critical thickness. The exact point depends on existing substrate dislocation geometry and kinetic barriers to dislocation glide and are not well understood at this time.

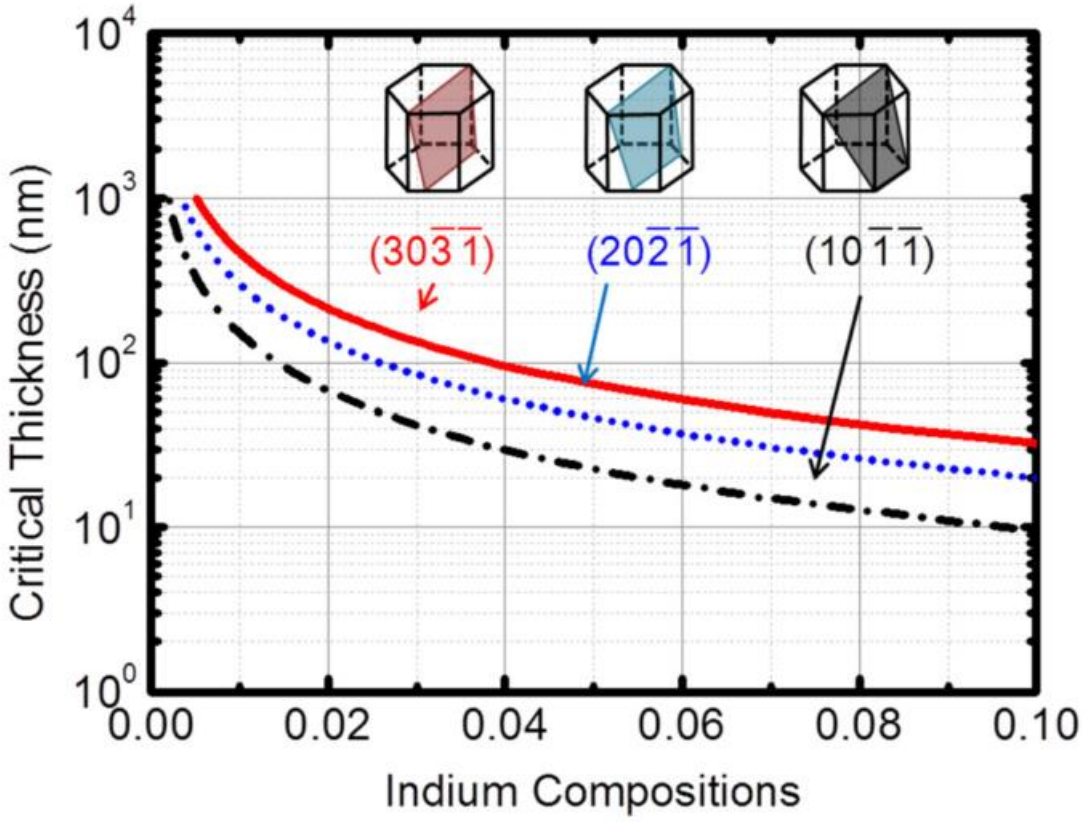

Figure 2-3: Critical Thickness for Semipolar Planes (Reproduced with the permission of AIP Publishing).[21]

Additionally, other slip systems exist including prismatic slip on inclined m-planes. If more strain must be relaxed, these other slip systems can be activated. This must be taken account in designing the growth. If relaxation occurs, the additional dislocations can act as nonradiative recombination centers. So, the thickness of InGaN and AlGaN layers must be limited. These

specific considerations and effects will be discussed in later chapters. Methods exist of engineering this relaxation, but this is beyond the scope of this dissertation. [9], [22], [23]

E. Semipolar p- (Al, In, Ga) N growth

Layers which are also found in any device and form the topmost layer of all devices in this dissertation are p-type GaN. The development of p-type GaN is widely regarded as a key breakthrough responsible for all GaN devices and was cited by the Nobel Committee in the awarding of the 2014 Nobel Prize for Physics.

Low resistance p-GaN is notoriously difficult to obtain. A few key issues related to p-GaN are described here. The p-layers are usually grown in hydrogen, which assists in the incorporation of the p-type dopant, Mg (source Bis(cyclopentadienyl)magnesium [Cp_2Mg]) by the formation of Mg-H complexes.[2] These complexes also result in the passivation of the magnesium acceptor, and a post growth thermal anneal in ambient gas is necessary to drive out the hydrogen and obtain p-type GaN.[24], [25]

The first p-type layer grown is usually the electron blocking layer. In most devices described in this dissertation, this is the only layer containing AlGaN, grown with TEG or TMG and trimethyl aluminum (TMA). AlGaN is used due to its increased bandgap compared to GaN, which will provide confinement for electrons and prevent them from escaping- hence the name electron blocking layer.

[2] The notable exception to this is p-InGaN which is usually not grown in hydrogen because the hydrogen ambient will etch the InGaN quickly.

F. Semipolar Indium and Impurity Incorporation

Growth on certain semipolar planes afford certain advantages and disadvantages besides polarization. Certain planes such as the ones discussed in this dissertation including $(20\bar{2}1)$, $(30\bar{3}1)$, $(20\bar{2}\bar{1})$ and $(30\bar{3}\bar{1})$ are not naturally occurring and can only be created by cutting a GaN substrate to expose a certain plane. When growth proceeds on planes such as $(20\bar{2}\bar{1})$ and $(30\bar{3}\bar{1})$, nanofaceted features are formed as can be seen in TEM[26] as seen in Figure 2-4.

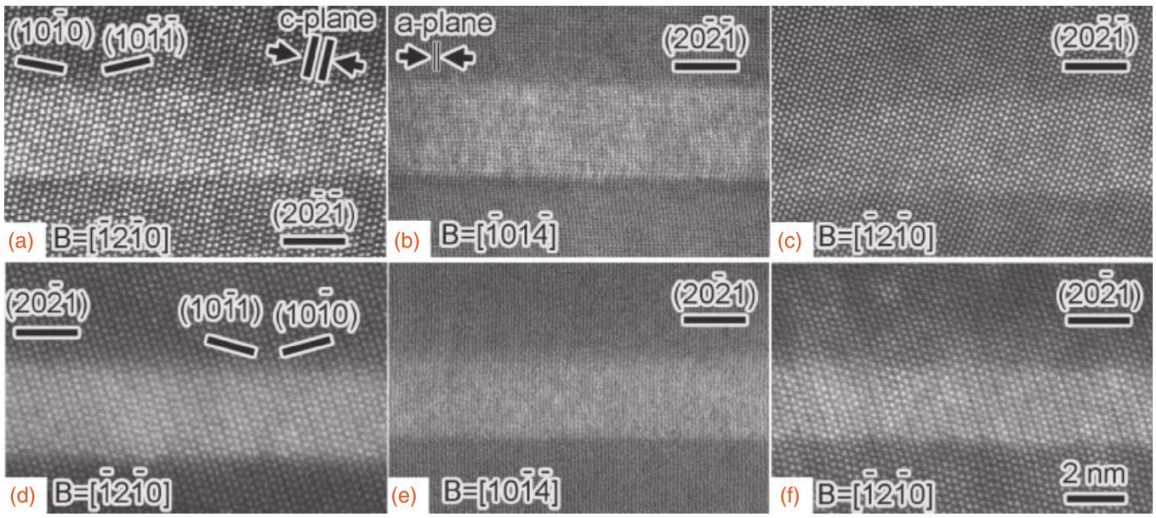

Figure 2-4: Nanofacet Semipolar Growth Reproduced with the permission of AIP Publishing. [26]

This feature of semipolar growth leads to interesting properties. First, these planes show high indium incorporation compared to c-plane.[27] This allows growth of InGaN layers at higher temperatures leading to improved crystal quality. Second, these planes also show higher impurity incorporation than c-plane. These impurities can cause dopant compensation or reduced conductivity.

G. Summary

The growth of semipolar (Al, Ga, In)N was reviewed. Semipolar growth is different from c-plane in several key ways. The template conditions must be optimized, and the ternary alloys must be carefully grown to avoid relaxation. Dopant and impurity incorporation for both p- and n-type semipolar (Al, Ga, In)N was also discussed.

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3. $(30\bar{3}\bar{1})$ High Power Low Droop Violet LEDs for Solid State Lighting

A. LED droop

As previously mentioned, the efficiency of conventional (Al, Ga, In)N-based light-emitting diodes (LEDs) grown on the polar *c*-plane drops dramatically at high current densities. This problem, known as efficiency droop, presents significant challenges to the fabrication of high power and high efficiency devices.[1], [2] The droop effect is further exacerbated for the thin (2~3 nm) quantum wells (QWs) used in conventional *c*-plane devices—a device structure used to compensate the low electron-hole wavefunction overlap and quantum confined Stark effect (QCSE) due to polarization.[3] This leads to an increased current density in the active region and a further increased droop effect on *c*-plane devices. More complex structures such as InGaN/GaN multiple-quantum-wells (MQWs) have been utilized to enhance the efficiency and reduce the droop on *c*-plane devices.[4] However, the results are not satisfactory due to the issues such as carrier transport, non-uniform carrier distributions in the wells, and still present polarization-related effects. Additionally, the phenomenon of thermal droop, where the external quantum efficiency (EQE) of devices decreases with increasing temperature, while less studied than current droop, is also an issue for nitride LEDs.[5],[6]

Alternatively, growth on nonpolar or semipolar planes of GaN holds great promise for high performance LEDs, due to the reduction of the polarization fields and the QCSE. Certain semipolar devices have already shown improved performance with reduced efficiency droop. For example, LEDs grown on the semipolar $(20\bar{2}\bar{1})$ plane have been demonstrated with low efficiency droop up to 400 A/cm^2.[7] It was argued that the low polarization-related electric fields and high-quality InGaN layer allows for LED structures with a relatively thick active layer, which are favorable for reducing efficiency droop. The carrier density dependent Auger recombination effect, recently shown to be a primary contributor to droop[8], [9] should be reduced for these thicker active layers. Additional advantages including high optical polarization ratio, high indium incorporation, small wavelength shift and narrow spectral linewidth were also reported for semipolar $(20\bar{2}\bar{1})$ LEDs and lasers.[10] However, more radical device structures and material advances are required to further improve the device performance.

B. Experimental Procedure for Development of High Power Low Droop $(\mathbf{30\bar{3}\bar{1}})$ *LEDs*

In this chapter, high power and low droop violet InGaN LEDs fabricated on the semipolar $(30\bar{3}\bar{1})$ plane, which is a semipolar plane with high inclination angle (100°) with respect to *c*-plane, are described. The low polarization-related effects and large critical thickness on the $(30\bar{3}\bar{1})$ plane enabled radical LED structures with very thick InGaN active layers, including single-quantum-wells (SQWs) and double heterostructures (DHs) with thickness ranging from 10 to 100 nm. Experimental results for both current droop and thermal droop are presented for LEDs with different active layer thicknesses. A high-performance low-

droop small-area (0.1 mm^2) semipolar $(30\bar{3}\bar{1})$ LEDs with over 1 W of light-output-power (LOP) at current density of 1 kA/cm^2, using this thick active layer design is reported.

LED structures were grown by conventional metal organic chemical vapor deposition (MOCVD) on free-standing $(30\bar{3}\bar{1})$ GaN substrates supplied by Mitsubishi Chemical Corporation. The device structure consisted of a 1 μm Si-doped *n*-type GaN layer, a ten-period Si-doped InGaN/GaN 3 nm/3 nm superlattice, a 15 nm thick lower GaN barrier, an InGaN active region with various layer thickness ranging from 10 nm to 100 nm, a 10 nm thick upper GaN barrier, a 16 nm Mg-doped $Al_{0.15}Ga_{0.85}N$ electron blocking layer (EBL), and a 60 nm *p*-type GaN layer. For the LED device fabrication, a rectangular mesa pattern (active area of $0.1mm^2$) was formed by conventional lithography and chlorine-based inductively coupled plasma (ICP) etching after an indium tin oxide (ITO) current spreading layer was deposited by electron beam evaporation. Ti/Al/Ni/Au n-type contacts and Cr/Ni/Au *p*- and n-pads were deposited by electron beam evaporation and a conventional lift-off process. The back side of the devices were roughened using a procedure published elsewhere.[11] The devices were then diced and mounted on a silver header and encapsulated in silicone.

C. Simulation of LED Structures: Band Diagrams and Relaxation

Figure 3-1 demonstrates the calculated band diagram profiles for violet *c*-plane and $(30\bar{3}\bar{1})$ LEDs with a 10 nm thick $In_{0.12}Ga_{0.9}N$ active layer at a current density of 100 A/cm^2, using the commercial SiLENSe package developed by the STR Group. The potential distributions were calculated by solving the Schrödinger-Poisson equations self-consistently and include strain and polarization effects. For the *c*-plane InGaN/GaN devices, it is well understood that due to the large polarization-related electric fields, the electrons and holes in

the active region will be pushed apart in opposite directions, which results in a distorted energy band diagram profile, a low electron-hole wavefunction overlap, and subsequently a low radiative recombination efficiency. For semipolar $(30\bar{3}\bar{1})$ devices, on the other hand, the polarization-related electric fields are much smaller than the *c*-plane case and a flat band diagram profile with high electron-hole wavefunction overlap can be obtained. It is noteworthy that this low wavefunction overlap problem will become more prominent for *c*-plane structures with increased active layer thickness, while the semipolar $(30\bar{3}\bar{1})$ structures can maintain a high wavefunction overlap (> 0.9) with very thick active layers.

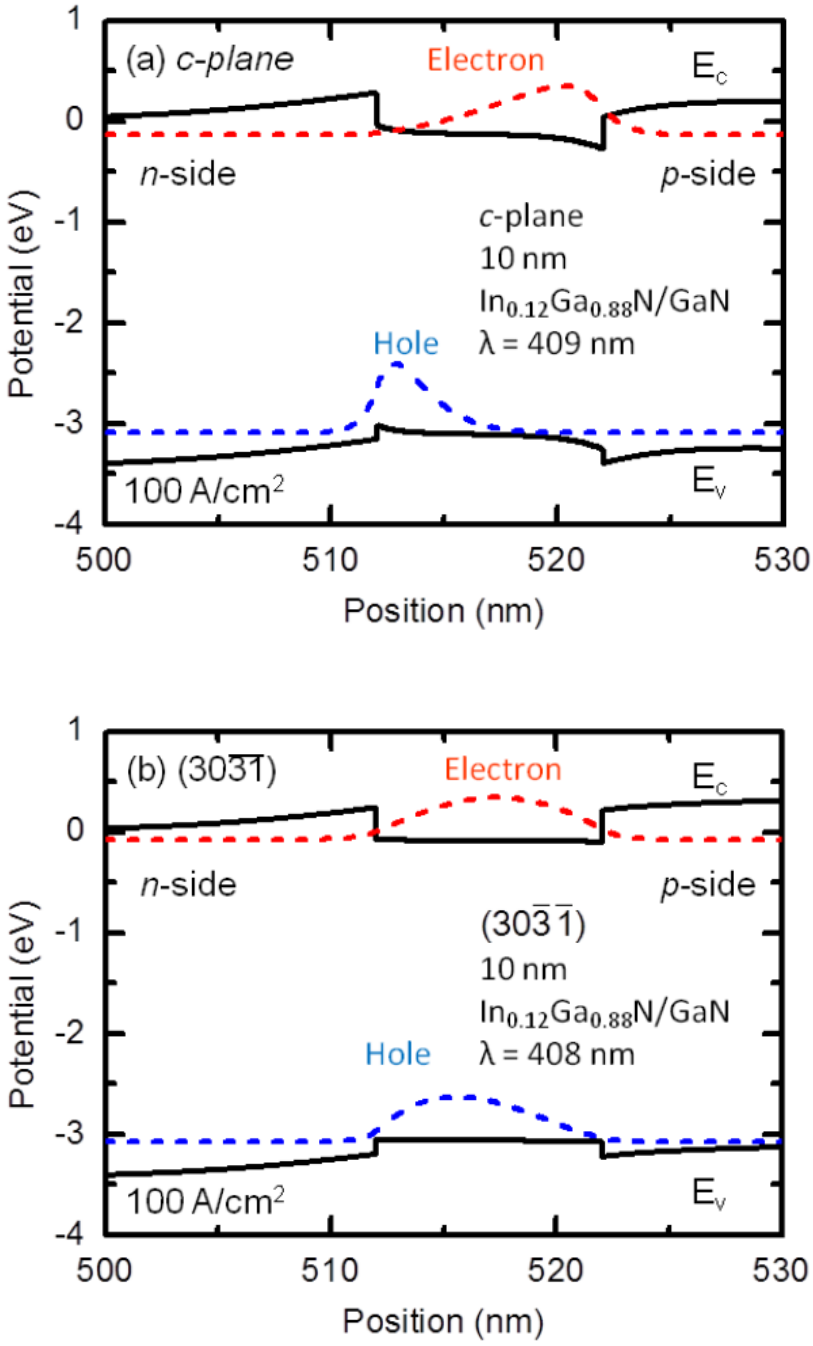


Figure 3-1: Band Diagrams for Thick SQW LEDs Reproduced with the permission of AIP Publishing.[12]

Figure 3-2 presents the Matthews–Blakeslee equilibrium critical thickness values (calculated under the assumption of isotropic elasticity) for InGaN layers on various semipolar planes. Growth of thick strained heterostructures on nonpolar and semipolar planes often leads

to the formation of misfit dislocations (MDs) at heterointerfaces via dislocation glide on the available slip planes.[13] The driving force for such dislocation glide originates from the resolved shear stress on the slip plane. Since the preferred slip plane in wurtzite GaN is the basal *c*-plane, this is referred to as basal plane (BP) slip. The resolved stress first increases with inclination angle from c plane to a maximum at about 45°, then decreases with increasing inclination angle from the *c*-plane, as shown in Figure III-2. Therefore, semipolar planes with high inclination angles (with respect to *c*-plane) such as the $(30\bar{3}\bar{1})$ plane will have an increased critical thickness for strained InGaN layers compared to other planes (Fig. III-2), due to the reduction in the resolved shear stress on the basal plane. Relaxation has been observed both above and below this calculated thickness.[14]

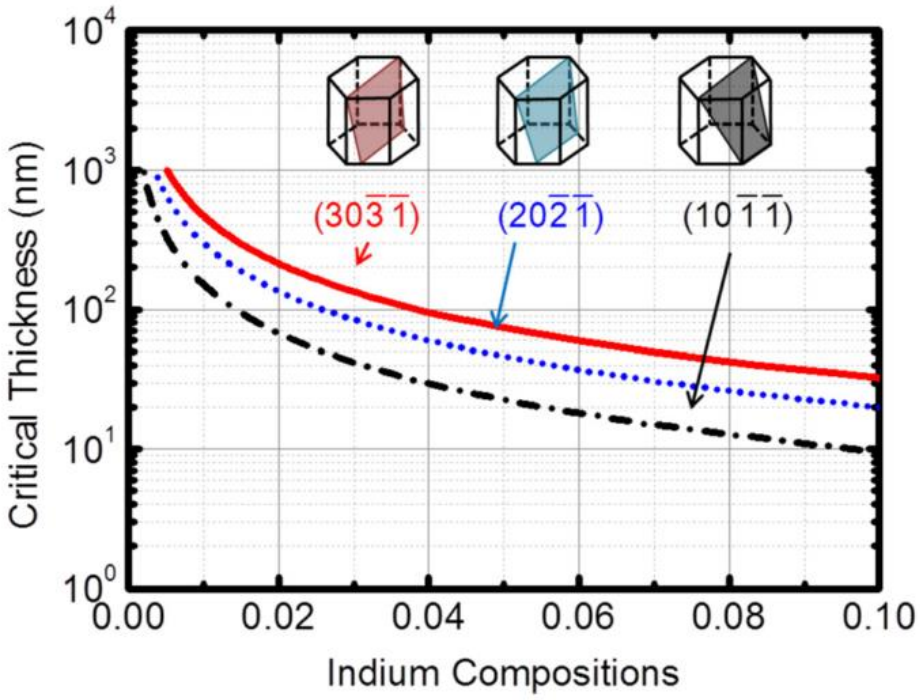


Figure 3-2: Critical Thickness versus Indium Composition for Various Semipolar Planes Reproduced with the permission of AIP Publishing.[12]

Kinetic factors such as Peierls barriers and/or existing threading dislocation geometries are suggested to be possible causes of this. Additionally, relaxation along other planes besides the basal *c*-plane has been observed. The activation of these other slip systems, referred to as 2D relaxation or non-basal plane (NBP) slip, can depend on those same kinetic factors that cause the deviation from the calculated basal plane relaxation critical thickness, and are also plane dependent.[15]–[17] The misfit dislocations caused by these non-basal plane slip systems can have a more dramatic effect on device performance, as shown below.

Figure 3-3 shows the electroluminescence light-output power as a function of active layer thickness for full LED structures grown on $(20\bar{2}\bar{1})$ and $(30\bar{3}\bar{1})$ planes. At low active layer thickness, the $(20\bar{2}\bar{1})$ LEDs showed comparable performance with $(30\bar{3}\bar{1})$ devices. When the InGaN layer exceeds its critical thickness (~20 nm), however, the $(20\bar{2}\bar{1})$ device performance drops dramatically. In contrast, the $(30\bar{3}\bar{1})$ LEDs showed higher performance with thicker active layer structures than the $(20\bar{2}\bar{1})$ devices due to the higher critical thickness. The optical performance of the devices was further illuminated by cathodoluminescence. Figure 3-4 (a)–(f) shows representative panchromatic cathodoluminescence (CL) images demonstrating the progression of defect generation and stress relaxation in $(20\bar{2}\bar{1})$ and $(30\bar{3}\bar{1})$ devices. (a)-(c) show Panchromatic CL images of $(20\bar{2}\bar{1})$ LED structures for 20, 40, 60 nm thick active regions, respectively. The circles in (a) highlight small NBP misfit dislocations. (d)-(f) show Panchromatic CL images of $(30\bar{3}\bar{1})$ LED structures for 20, 40, 60 nm thick active region. At 20 nm, a few dark lines parallel to the *a*-direction (BP MDs) are visible for the $(20\bar{2}\bar{1})$ devices. Very small NBP MDs can be seen, indicating the onset of performance-degrading 2D relaxation. Starting from 40 nm, a significant amount of non-basal

plane dark defects are seen on $(20\bar{2}\bar{1})$ devices, indicating that the InGaN layers were experiencing stronger 2D relaxation as the thickness increased, corresponding to the low output power. The $(30\bar{3}\bar{1})$ structures showed similar trends with $(20\bar{2}\bar{1})$ devices. However, due to the increased critical thickness, no NBP MDs can be seen on the 20 nm image, and significantly fewer NBP MDs for 40 nm and 60 nm cases. This indicates that the $(30\bar{3}\bar{1})$ samples were less relaxed compared to $(20\bar{2}\bar{1})$ devices, and it also indicates that BP misfit dislocations do not have a large impact on device performance, especially for thick InGaN layers. This is consistent with the device results in Figure 3-3.

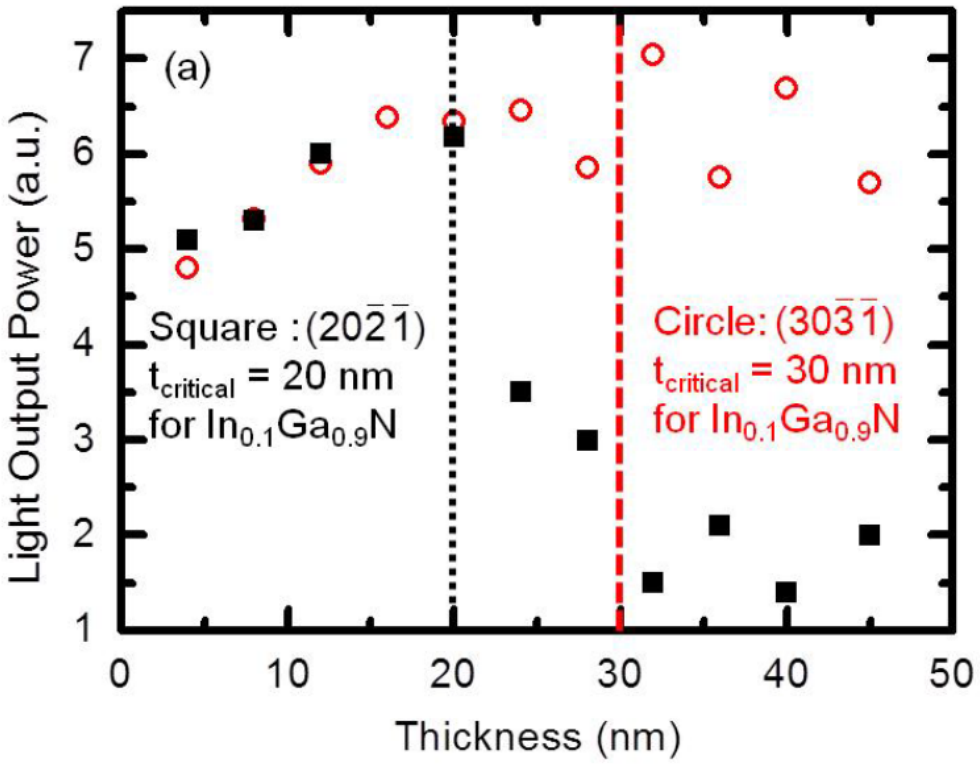


Figure 3-3 Electroluminescence Light Output Power versus Thickness of QW/DH. The MB critical thickness is overlaid for each plane. Reproduced with the permission of AIP Publishing.[12]

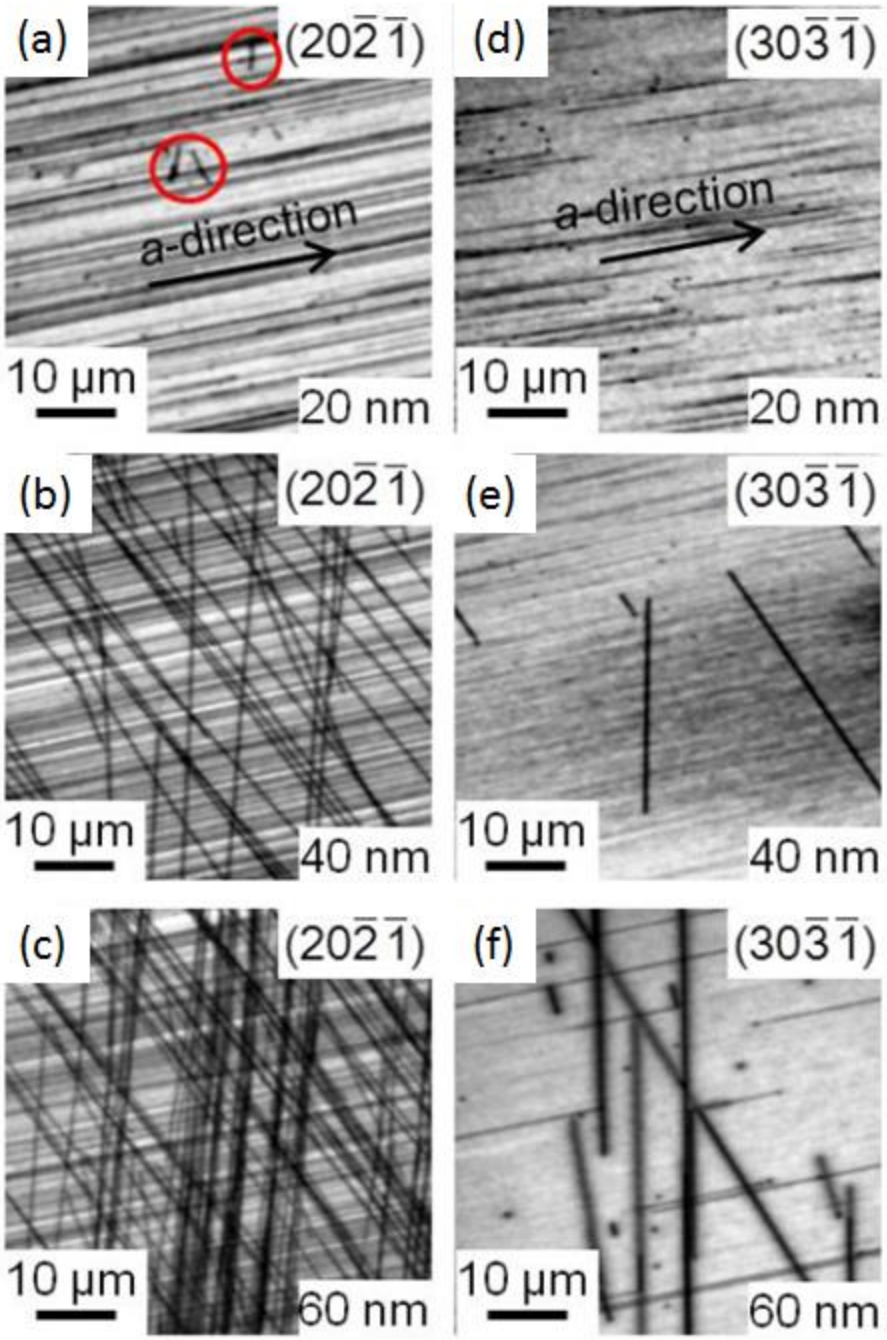


Figure 3-4: Misfit Dislocation Evolution Reproduced with the permission of AIP Publishing.[12]

D. Results of High Power Low Droop $(30\bar{3}\bar{1})$ *LEDs*

Figure 3-5(a) presents the external quantum efficiency (EQE) as a function of current density for $(30\bar{3}\bar{1})$ LEDs with various active layer thicknesses under pulsed operation (1% duty cycle). The LEDs with the lowest InGaN thickness (10 nm) showed the highest peak efficiency. The peak efficiency decreases with increasing active region thickness, and also is shifted to higher current densities. Figure 3-5(b) shows the same data plotted with normalized EQE versus current density on a logarithmic scale. The data in this figure shows a trend with lower EQE droop with increasing active region thickness.

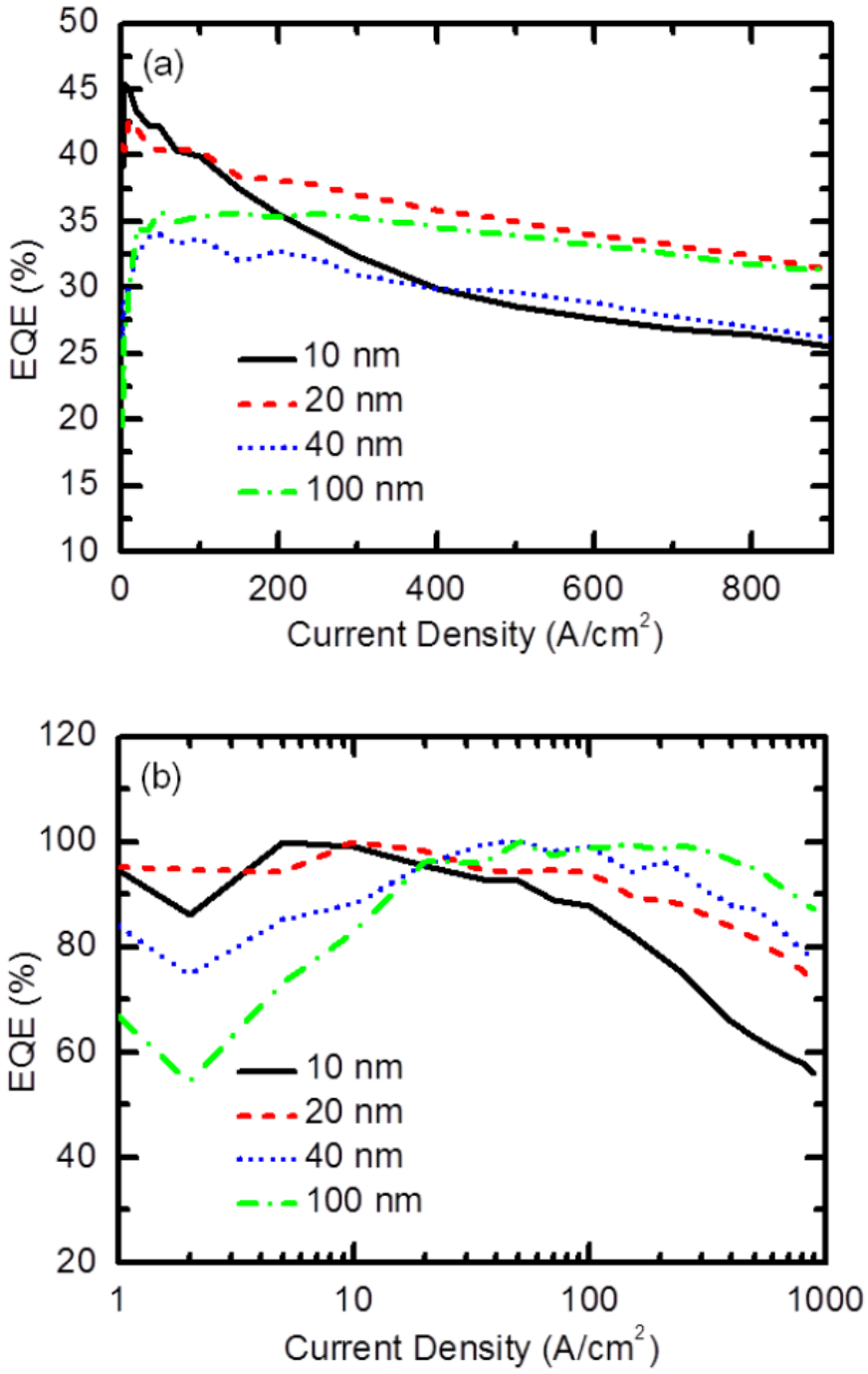
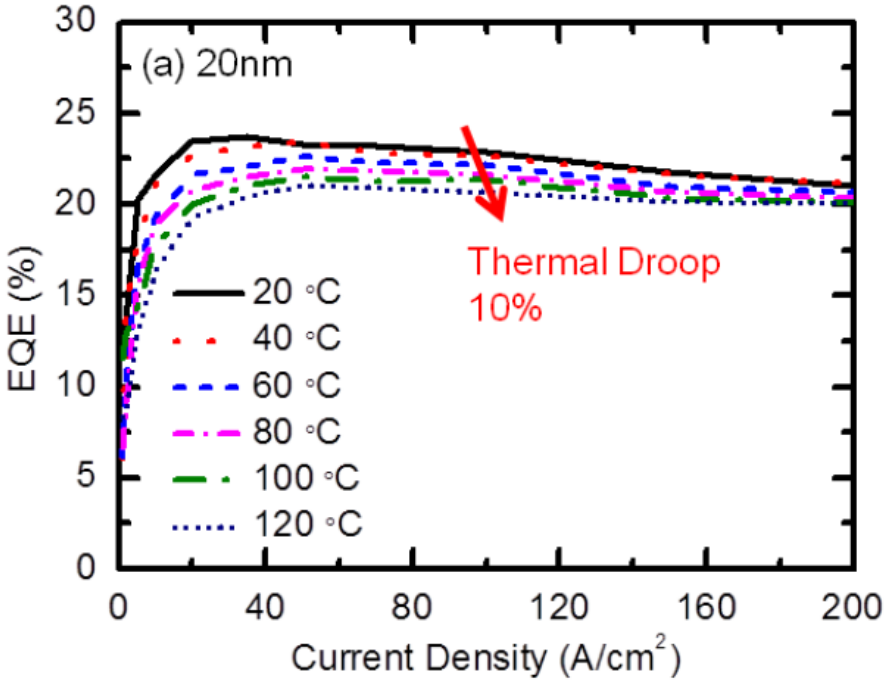


Figure 3-5(a) Absolute EQE versus current density and (b) Normalized EQE versus current density on a logarithmic scale for LED devices with active region thickness 10-100 nm (Pulsed condition, 1% duty cycle). Reproduced with the permission of AIP Publishing.[12]

Figure 3-6 shows EQE versus current density at different device temperatures. A decrease can be seen in EQE as the temperature increases as has been identified elsewhere.[6] This is termed thermal droop. In order to quantify the thermal droop, a factor known as the hot/cold (H/C) factor is used. This is defined as: hot/cold factor = $EQE_{100\,^{\circ}C}$ / $EQE_{20\,^{\circ}C}$. The devices with relatively thin active regions (10 to 40 nm) showed improved thermal characteristics with only 10% EQE droop at 120° C, corresponding to an H/C factor of 0.9, similar to that of devices with thick active regions on the $(20\bar{2}\bar{1})$ plane. Figure 3-6(a) shows a representative curve for the 20 nm thick active region device. As the active regions became thicker, the thermal performance suffers. Figure 3-6(b) shows the performance of the 100 nm thick active region device, which showed 20% EQE droop at 120 °C (H/C factor of 0.8).


(a) 20nm
EQE (%)
Current Density (A/cm^2)
Thermal Droop
10%
20 °C
40 °C
60 °C
80 °C
100 °C
120 °C
0
5
10
15
20
25
30
0
40
80
120
160
200

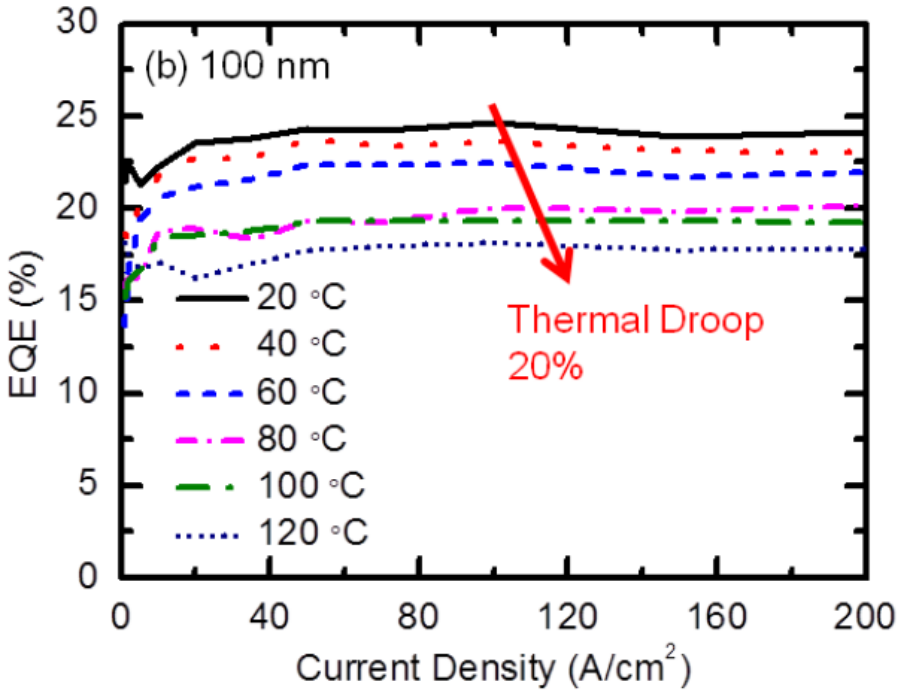


Figure 3-6 EQE versus current density measured at different temperatures for devices with a (a) 20 nm thick active region and (b) 100 nm thick active region. Reproduced with the permission of AIP Publishing.[12]

The above studies were used to optimize a device structure to obtain the highest performance. An active layer thickness of 15 nm was selected and a device was fabricated as discussed above, but packaged using a vertical transparent packaging method.[11] Figure 3-7(a) shows the EQE and LOP of the small-area 0.1 mm^2 LED device under pulsed operation (1% duty cycle). A peak EQE above 50% drooping to only 33% at a current density of 1 kA/cm^2 and power of 1008.7 mW at 1 kA/cm^2 is shown. Figure 3-7(b) shows the wavelength and full width at half maximum (FWHM) of the emission spectrum. A very small wavelength shift of only a few nm up to 1 kA/cm^2 and a low FWHM were present.

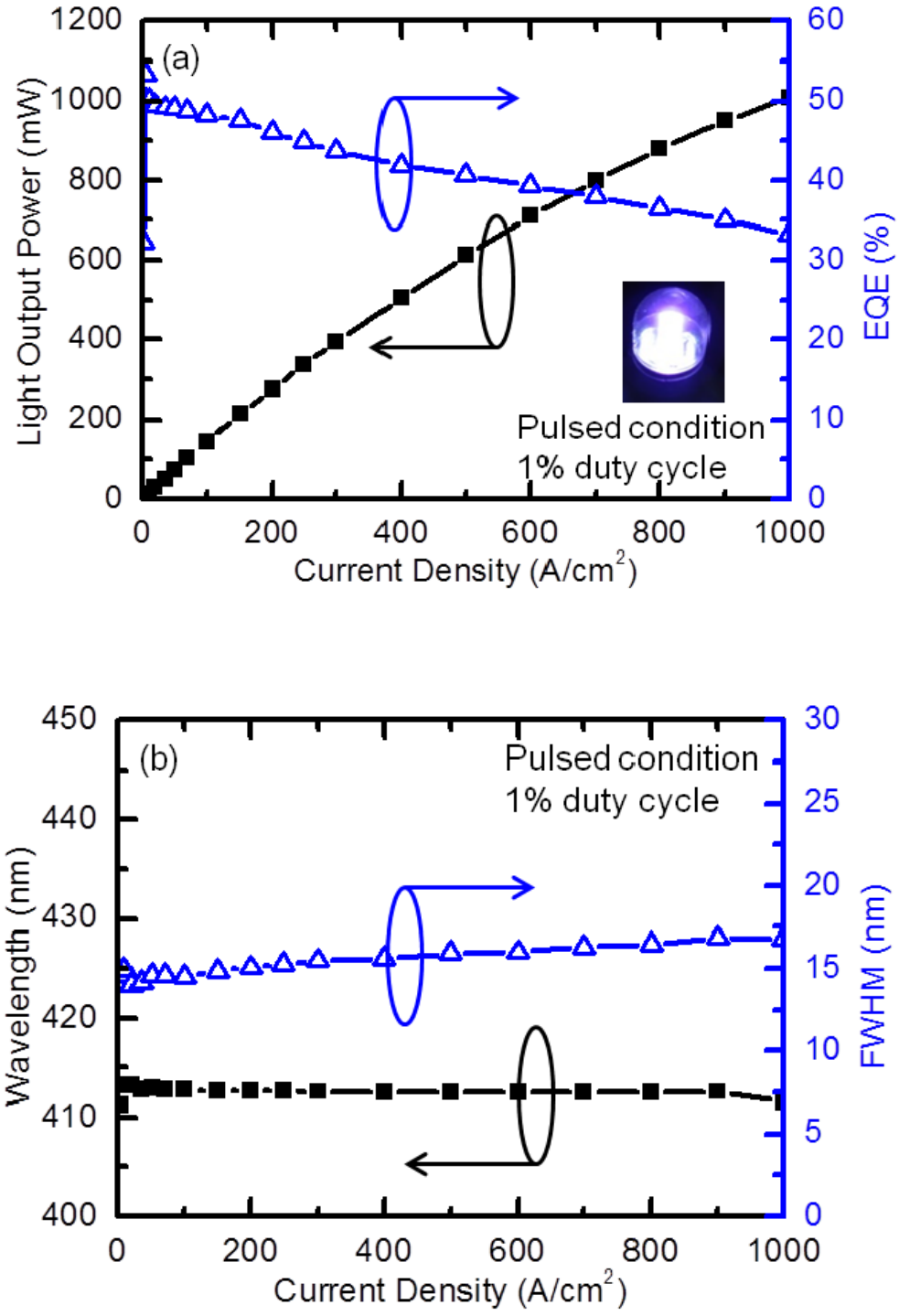


Figure 3-7 (a) Output power and EQE versus current density for packaged LED device with a 15 nm thick SQW active region (Pulsed condition, 1% duty cycle). (b) Peak wavelength and FWHM for the device as a function of current density. Reproduced with the permission of AIP Publishing.[12]

E. Conclusion

In summary, LED devices with very thick active regions of 10-100 nm were grown on the $(30\bar{3}\bar{1})$ plane of GaN. Utilizing the low polarization fields and high critical thickness of this plane, high power low droop LEDs were fabricated. Electroluminescence and cathodoluminescence confirmed fewer 2D dislocations on $(30\bar{3}\bar{1})$ devices led to higher performance at very thick active regions. A trend in lower droop with thicker active region thickness was demonstrated. The results of this study led to the fabrication of a small-area 0.1 mm^2 LED with over 1 W of output power at 1 kA/cm^2.

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4. Laser Diode Design

A. Motivation

In the last chapter, one method of improving efficiency of solid state lighting at high current density was presented. Since Auger recombination is intrinsic to GaN, droop cannot be eliminated fully in LEDs. However, by moving to laser-based lighting, one can obtain high power devices with very low device footprint and high brightness at high current density. Auger processes clamp at laser threshold, so beyond threshold the EQE will increase.

Laser-based lighting has been discussed in several works.[1]–[4] The next few chapters will focus on improving the LD used as source for lighting. This chapter introduces laser growth and laser design considerations.

B. Baseline High Power $(20\bar{2}\bar{1})$ *Laser Design*

Compared to LEDs, certain additional features must be considered when designing the epitaxial structure of LDs. Earlier chapters described many of these issues; they will be reviewed here in a systematic way, using the epitaxial structure developed by Pourhashemi and Farrell et al.[5] as a guide. Figure 4-1 shows this structure.

The substrate for the high power LDs was $(20\bar{2}\bar{1})$, chosen because of the high indium incorporation, low polarization fields, and low wavelength shift demonstrated on devices grown on this plane.[6], [7] The epitaxial structure consisted of a 1-μm *n*-GaN cladding, followed by a 10-nm linear composition grade from *n*-GaN to *n*-$In_{0.06}Ga_{0.94}N$, a 50-nm *n*-

$In_{0.06}Ga_{0.94}N$ waveguiding layer, and another 10-nm linear grade back down to the first GaN barrier. The active region consisted of an undoped 4-period InGaN/GaN (3.5 nm / 7 nm) multiple quantum well (MQW) emitting at about 440 nm followed by a 12-nm *p*-$Al_{0.18}Ga_{0.82}N$ electron blocking layer, which was then linearly graded in composition over 10 nm to *p*-GaN. The *p*-type waveguiding layer followed with the same composition grading and thicknesses as in the *n*-type waveguiding layer. The *p*-GaN cladding was 650 nm thick and capped with a *p*++ contact layer. The compositional grades are designed to limit voltage drop at the heterointerfaces. By introducing a compositional grade, the band diagram will be smoothed out near the interface and no sharp barrier to charged carrier flow will be present. The waveguiding layers of $In_{0.06}Ga_{0.94}N$ are selected to provide confinement, but the indium composition must be kept low enough so as to not absorb and of the light from the active region. Sub-bandgap absorption may be an issue with these layers, it may be explored if future work. The p++ contact layer must be carefully engineered to obtain an ohmic contact, this will be discussed in several areas later in the dissertation. The doping and composition of the EBL must be carefully selected to create a barrier to electron overflow but no impedance to hole injection. The doping in the EBL is usually kept higher than the doping in the p-type layers on either side for that purpose. The details of fabrication including the contacts will be described in the next chapter.

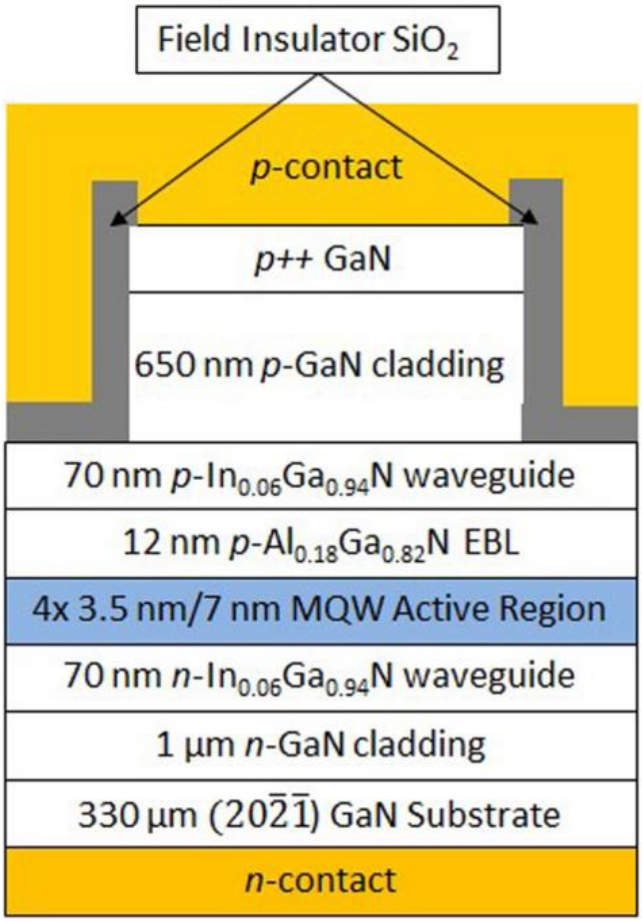

Figure 4-1: Cross-section of Starting Laser Structure Reproduced with the permission of AIP Publishing.[8]

When designing the laser- it is important to consider the confinement of carriers and photons. Confinement of photons is accomplished by sandwiching layers of lower refractive index on either side of the active region, forming an optical cavity. Using the transfer-matrix method, the electric fields and thus the profile of the fundamental mode of this cavity can be calculated, as can be seen in Figure 4-2 as the black dashed line. The confinement factor, defined as the overlap of the mode with the quantum wells- in this design is 3 %.

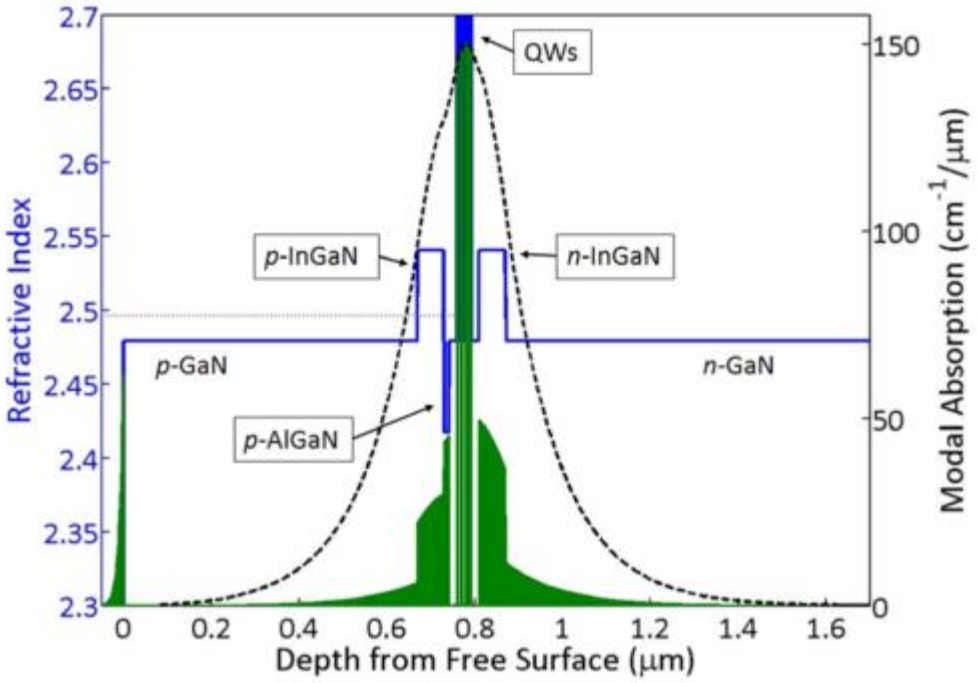

Figure 4-2: Waveguide Design for Baseline Laser Reproduced with the permission of AIP Publishing.[8]

The green shaded areas represent absorption losses in the structure due to absorption by dopants or free carriers, etc. This will be discussed in more detail in Chapter 4. A 2-D mode profile calculated from the commercial software FIMMWAVE is shown in Figure 4-3.

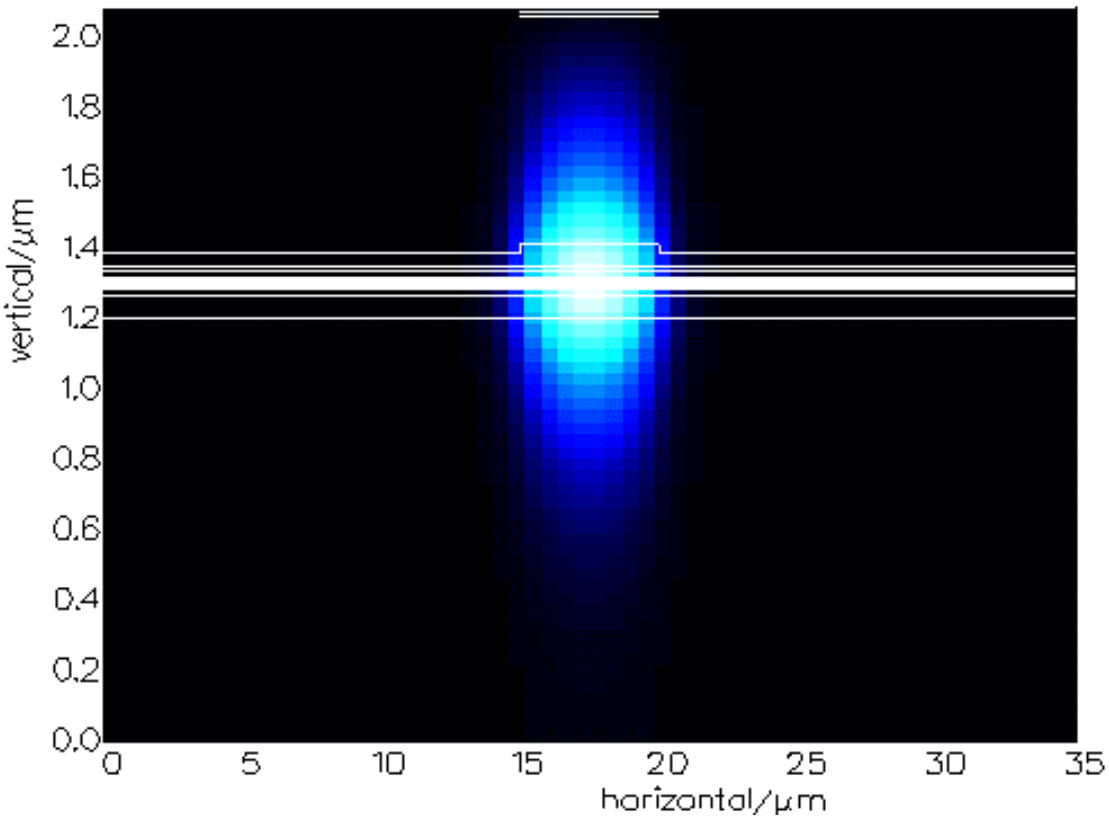

Figure 4-3: 2-D Mode profile for baseline laser

C. Case Study: Coupled Laser

A more advanced example of LD design is discussed in this section. This work suggests using a coupled laser, a monolithically integrated optically pumped and electrically injected LD. The section will describe the motivation and progress of the work in detail, and suggest ways of continuing this work, which is not described elsewhere in the dissertation.

This work suggests using optically pumped long wavelength emitters as opposed to electrically injected devices as a method for overcoming the above problems with green devices. The principle advantage of optically pumping devices in this context comes from the

much wider material design space that optical pumping allows. Since optical pumping relies on photogenerated carriers rather than injected carriers, carriers need not transport to the wells via injection. This overcomes the problem of low p-GaN conductivity and hole mobility, a well-studied phenomenon.[9],[10] The low hole mobility leads to poor hole injection into MQW structures and thus reduced efficiency if the barriers are too large.[11] With optical pumping, because carrier transport to the wells is not an issue, this allows for wider barriers between the wells to limit the overall strain in the structure. This could lead to improved material quality and better device properties.[12]

Another consequence of this wide design space is the ability to grow many quantum wells as a part of the active region. The strain can be managed as stated above by growing wide barriers. More quantum wells can lead to increased transverse confinement factor.[13] Of course, this can also increase the transparency carrier density, so attention must be paid to that balance. Another benefit is the fact that the p-type layers can be kept far away from the green wells. This limits the green mode overlap with the p type layers, which are known to be the largest source of loss in nitride LDs.[14],[15]

However, simply creating an optically pumped device is not desirable for an application in itself. Optically pumped devices that are externally pumped by another laser device require additional packaging and fabrication steps, and thus would be higher cost than an efficient electrically injected device. Therefore, it is desirable to integrate an optically pumped device with an electrically injected one in some fashion to take advantage of these benefits. There have already been demonstrations of using optically pumped long wavelength quantum wells as converter layers for LED devices. A group from OSRAM in 2011 discussed the use of 40-period c-plane quantum wells with similar luminous flux to electrically injected green

devices.[16] They demonstrated improved efficiency in 2013 working with a group at the University of Ulm, Germany.[17] Collaborations between OSRAM and Bhattacharya's group at Michigan investigated the use of red quantum dots grown by MBE as converting layers.[18] Additionally, Damilano et al demonstrated a similar idea using a blue pump and yellow converting layers grown by MOCVD.[19] This was investigated by Kowsz et. al. at UCSB. [20], [21] A recent analysis by Neuschl et al from the University of Ulm (working with OSRAM) suggested that semipolar planes show better optical excitation characteristics than c-plane devices due to the reduced polarization fields.[22]

A new device design can incorporate the best of both worlds: monolithically integrated optically pumped and electrically injected devices. This was originally conceived by Farrell, Weisbuch and Nakamura as outlined in a yet-unpublished patent. It can gain the benefits outlined above of optical pumping, while keeping the low form factor of a conventional electrically injected device. This work focuses on lasers, rather than LEDs, principally due to the laser lighting benefits outlined above but also because lasing from such a structure has not yet been demonstrated. There are several possible device designs that will be outlined in this section, before settling on one structure to test first. All of these designs use an electrically injected shorter wavelength laser (generally blue) to optically pump a longer wavelength laser, green to begin with. Since the lasing properties (material gain, wall plug efficiency) of blue lasers are generally much better than green lasers, this route is promising.[5], [23], [24]

Figure 4-4 shows two designs, referred to in this chapter as follows: Figure 4-4A, an Evanescently Coupled Laser (ECL), and Figure 4-4B, a Horizontal Cavity Surface Emitting Laser (HCSEL). These figures are taken from a patent filed by Farrell, Weisbuch, and Nakamura in 2015. The ECL design consists of two lasers grown on the same side of a $(20\bar{2}1)$

GaN substrate, where the blue mode overlaps the green mode to pump the green laser. The HCSEL design consists of a blue laser grown on a $(20\bar{2}\bar{1})$ substrate, with a green laser grown on the reverse of that substrate, a $(20\bar{2}1)$ side. Additional optical elements such as gratings and mirrors are added to direct the blue light towards the green laser. Each design has certain benefits and challenges associated with it and specific design requirements.

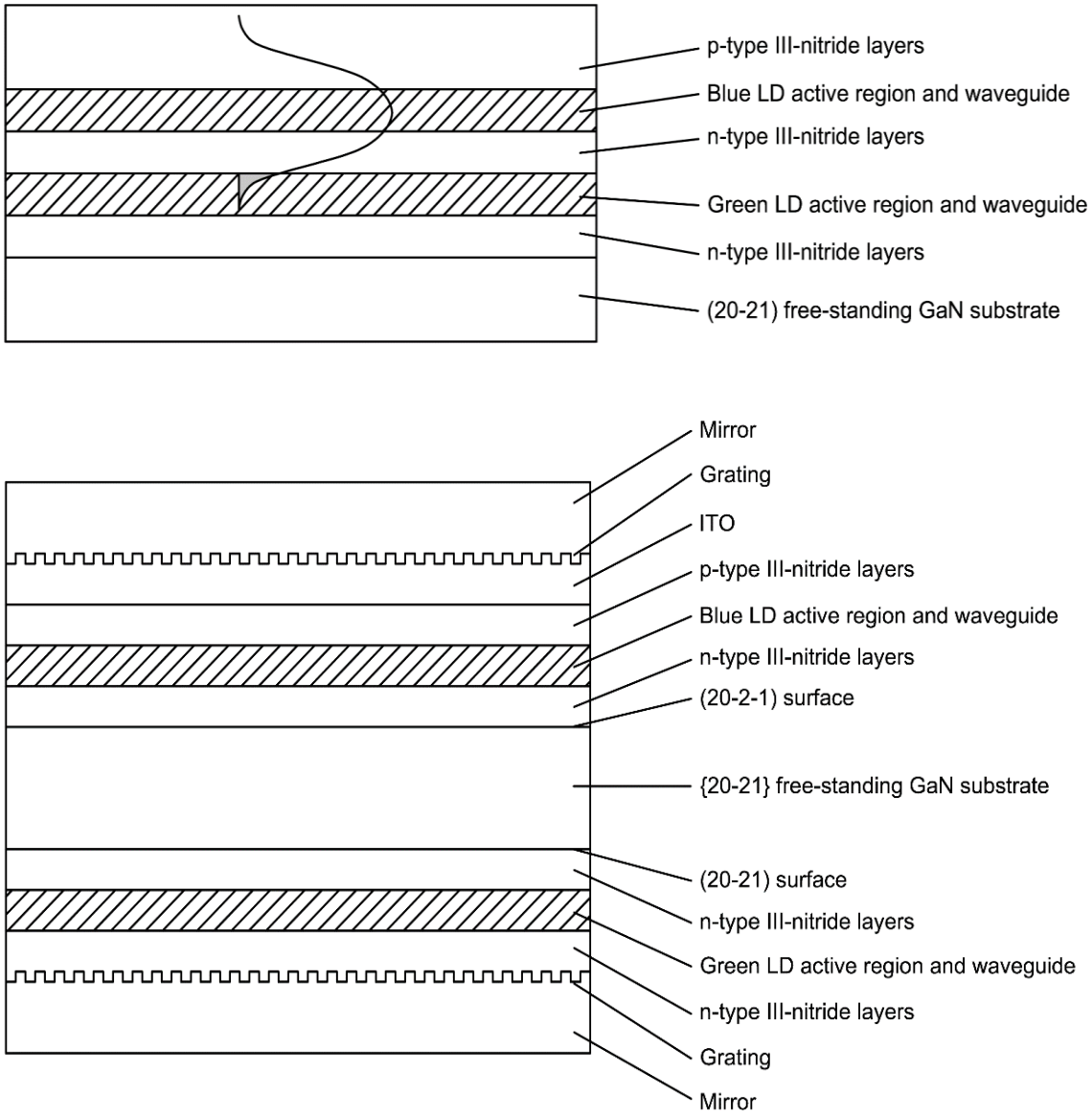

Figure 4-4: ECL and HCSEL Designs

The ECL design requires careful design of each layer. It is essential that the distance between the two lasers is chosen to promote successful coupling of the mode. It must be balanced between absorption in the green cavity and loss in the blue cavity. If the distance between the two is too great, there will be no mode overlap, and the green wells will not absorb enough light. If they are too close, there will be too much overlap and the blue laser will have too high a loss from the green wells and it will not lase. More details including mode simulations will be presented.

Additionally, the growth of blue lasers on $(20\bar{2}1)$ planes has so far lagged behind $(20\bar{2}\bar{1})$ planes.[5],[23] It is not clear if this is a fundamental issue related to the differences between the planes or if more optimization of $(20\bar{2}1)$ lasers are needed. Research into this will be presented in later chapters. Further, in order for the blue laser to be electrically injected, it must be grown after the green laser. This introduces the problem of thermal damage to the green wells during the growths of subsequent blue InGaN QWs, InGaN separate confining heterostructures (SCHs), and p- and n-type GaN cladding layers.

The HCSEL design has the advantage of utilizing the high performance $(20\bar{2}\bar{1})$ plane for the blue and the $(20\bar{2}1)$ plane for the green. However, it will take significantly longer to grow, since it will require growth on the opposite side of the substrate. This requires oxide passivation of the side not being grown on before growth. Additionally, the currently available double side polished (DSP) substrates have proven to have one side inadequately prepared for laser device fabrication with polishing defects present. Further, the design requires the fabrication of a second order grating. This will require a pitch size of approximately 180 nm

[25],[26] which requires electron beam lithography, a costly technique. Fabricating this in GaN may prove difficult as well, although this may be similar to previous photonic crystal work.[27] Additionally, mirrors must be used to direct the light downward which have proven difficult to fabricate.

The ECL design will be substantially easier to fabricate and test than the HCSEL design, and the growth will be quicker, requiring only one growth compared to two growths for the HCSEL. Since the goal of the project was to demonstrate a high efficiency green laser, an estimation of the relative efficiency of the two approaches was done based on state of the art coupled lasers. For the ECL design, if the mirrors on the facets are designed well, it is possible to obtain nearly 100% reflectivity. This will allow *all* of the light produced beyond threshold to be used to pump the green laser. Conversely, the HCSEL design will require coupling to a grating, shown to be relatively inefficient. So it was decided to pursue the ECL design.

First, the focus is placed on the ECL device design. An example of the calculated mode profile is shown in Figure 4-5. It consists of n-GaN template/cladding, an $In_{0.30}Ga_{0.70}N$ green active region between an $In_{0.08}Ga_{0.92}N$ separate confining heterostructure (SCH)[28], a spacer layer of GaN which was varied in thickness during the simulation, and then a standard blue laser structure. The red line is a mode which will not lase, and its parameters are not relevant. The results are presented in Figure 4-6. This figure summarizes three trends with spacer thickness, the confinement factor in the blue wells, their overlap with the green wells, and the loss in the blue waveguide mode. A suitable distance must be selected such that the loss in the blue wells (which will contribute to absorption in the green and thus optical pumping) will not be too high so as to stop the blue laser from reaching threshold, but not too low such that the

green laser will not reach threshold. In this model, the internal loss of the blue laser was set to be 20 cm^{-1}, so all loss above this point can be considered to be due to absorption in the green wells. With this assumption, a distance of 800-900 nm was selected. Figure 4-6 summarizes the results. Additionally, the 2D waveguide mode solver FIMMWAVE was also used to model this structure. It showed good agreement with the 1D simulation results, and that the green mode will remain confined despite a large distance from the ridge.

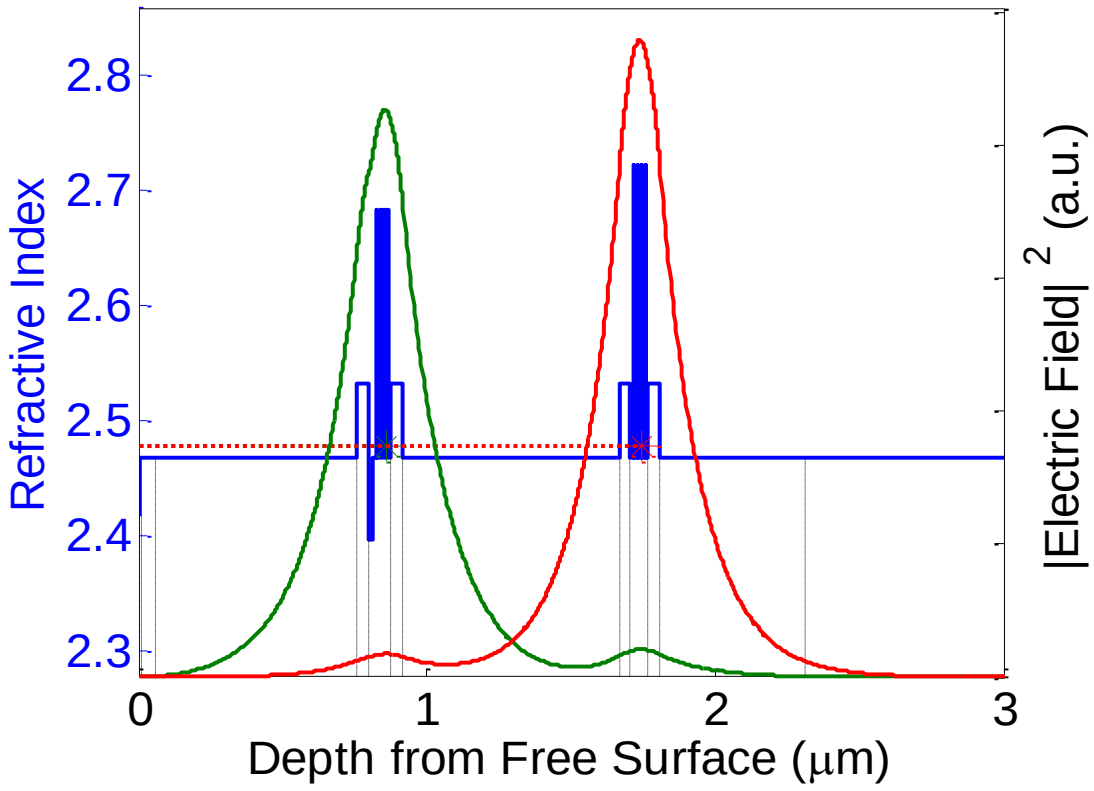

Figure 4-5: Example of Optical Mode Simulation where the two lasers a spaced 750 nm apart. The green line is the blue mode.

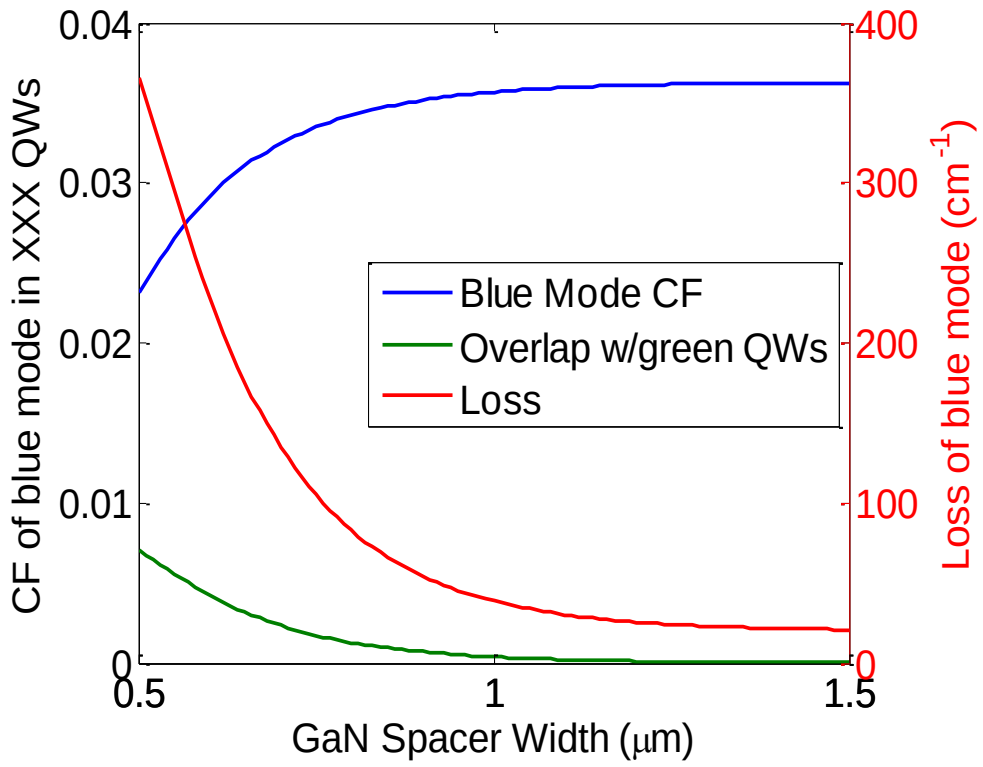

Figure 4-6: Summary of Blue Mode Simulation.

This structure was grown with the photoluminescence and electroluminescence/quicktest shown in Figure 4-7. The PL spectrum shows clear separate peaks at 458 nm and 515 nm as desired. The EL spectrum shows strong blue emission with a small green shoulder from low optical pumping. The power from the EL test was ~2 mW. This power was the same power as a blue laser structure grown in the run immediately after, showing that the blue laser growth on top of the green wells was of good quality. Additionally, AFM scans of a sample grown up to just before the blue SCH showed less than 1 nm RMS roughness and no dark triangle defects, indicating it was possible to grow good quality thick GaN at low enough temperature such that the green wells will not be damaged. Furthermore, no dark triangles were observed on the two-laser growth. In order to realize an integrated optically pumped structure, both electrons and

holes must be injected to the blue laser above the green wells- so a topside n contact design is required. The process flow is described in Chapter 5. The actual device fabrication met certain challenges that at time of writing have not been addressed, but future work is possible to realize this device.

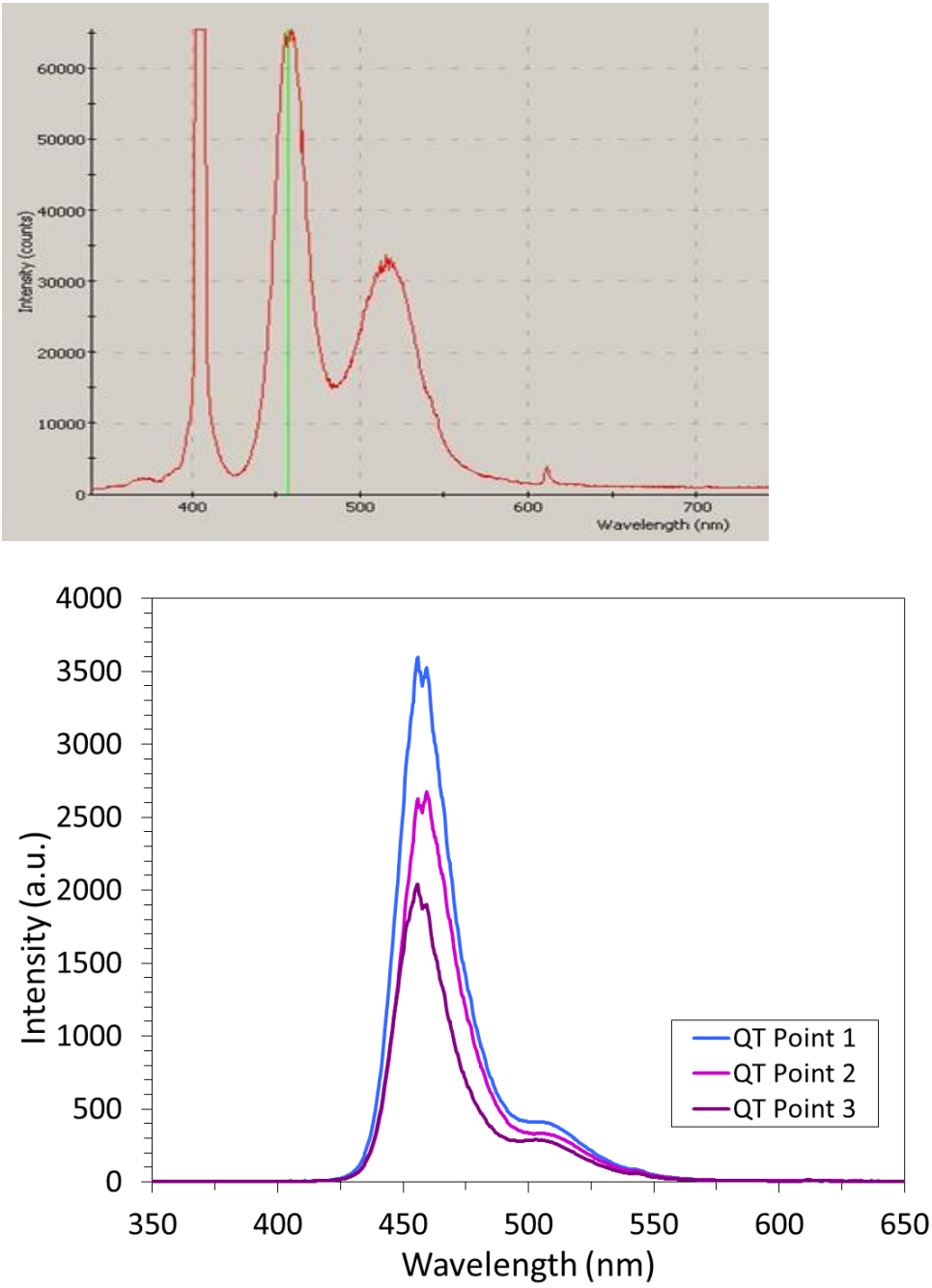

Figure 4-7: PL and EL of Double Laser Epi

D. Summary

Laser Design considerations were presented in this chapter. An overview of the baseline high power laser structure was presented, and a coupled laser design was discussed.

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5. Laser Fabrication

This chapter focuses on advances in edge emitting LD fabrication. Full descriptions of the various processes used are presented in Appendix A.

A. Baseline Laser Process: Self-Aligned Ridge, Backside n-contact

An overview of the LD process inherited from previous work will now be presented. This design used a self-aligned process to form a shallow ridge waveguide. The steps are as follows. First, the ridge is etched using Cl_2/BCl_3 reactive ion etching (RIE) and SiO_2 was blanket deposited as a field insulator and lifted off the ridges using a self-aligned process (one lithography step is used for both of the above steps). Then a p-contact of Pd/Au is deposited on top of the ridge using electron beam (e-beam) evaporation and liftoff. The mirror facets are etched using RIE, and then a backside contact of Al/Au is blanked deposited on the back. Figure 5-1 shows this process schematically. Details of the process are presented in the appendix.

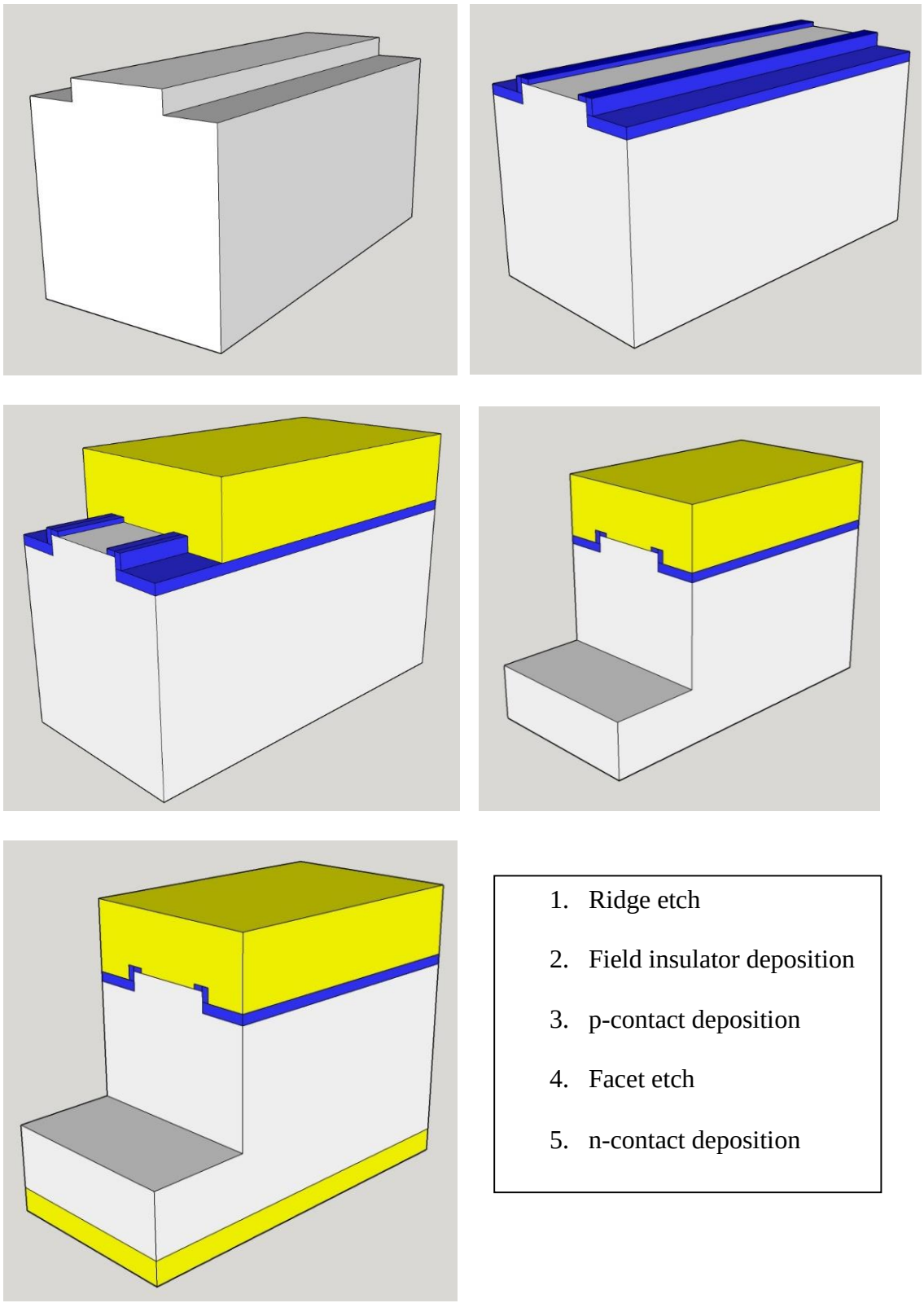


Figure 5-1: Baseline Laser Process

This process produced working lasers, but several issues remained that are addressed in the rest of this chapter.

B. p and n-contact Improvements to Baseline Laser Process

The baseline laser process includes one p-metallization step. This is problem because the Pd contact, while show to be a good contact to p-GaN, does not stick well to the field insulator SiO_2, so the pads would frequently peel off when subject to cleaning or heating during testing. To correct for this, an additional metallization step was added. A p-contact of Pd/Au is used, and then a p-pad of Ti/Au is deposited on top to completely cover the p-contact. No adhesions issues were encountered after this fix. Figure 5-2 shows this new laser in schematic form.

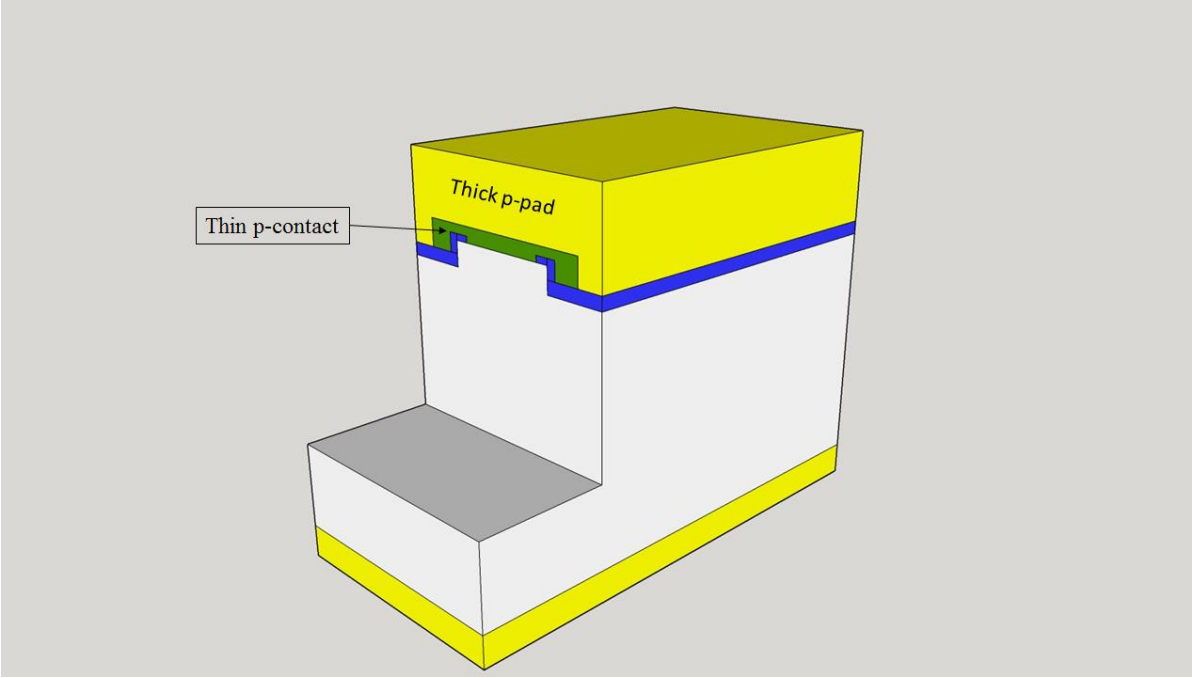


Figure 5-2: Laser with p-contact/p-pad fix

Other p-contacts can be used also. Transparent conductive oxides (TCOs) such as ITO[1] or ZnO[2] could be used as the p-contact instead of Pd. The devices presented in this dissertation did not use TCOs, but the appendix and future work sections will present fabrication details for ITO.

The backside n-contact also needed to be improved. A diffusion barrier of Ni was inserted between the Al and Au to maintain stability under testing.

C. p++ Layer Optimization

An important part of obtaining a good p-contact is the growth conditions of the p++ contact layer.[3] The growth conditions including V/III ratio (with NH_3 flow as proxy) and Mg doping (with Cp_2Mg flow as proxy) were investigated on $(20\bar{2}\bar{1})$ test structures. Figure 5-3 shows this result, where the highest current at constant applied voltage is obtained with NH_3 flow of 6 slm, grown with TEG 50 sccm and H_2 carrier gas. With NH_3 flow of 6 slm and Cp_2Mg flow at least 100 sccm, the best conditions were obtained. It is possible that annealing the p-contact could improve performance[4], [5], that is the subject of future work.

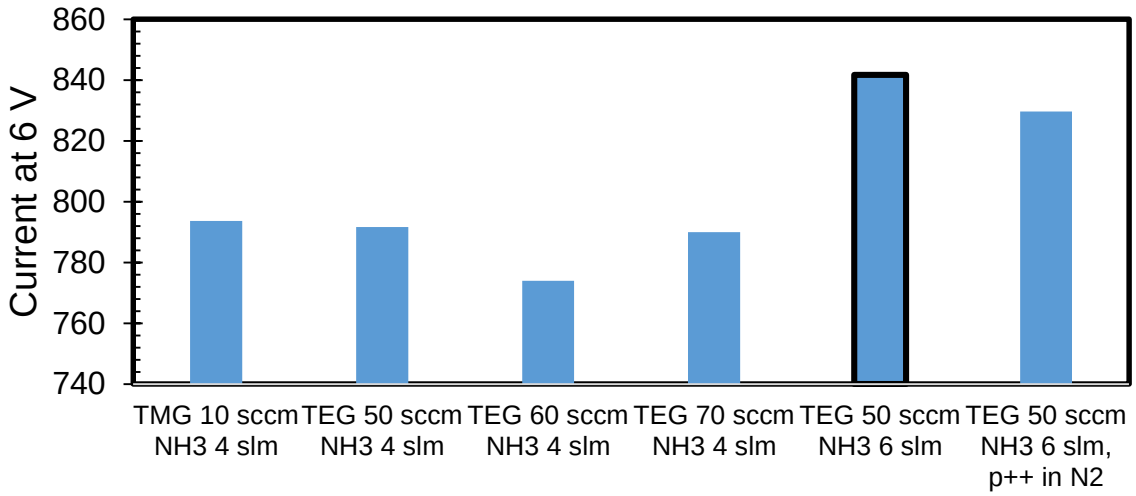


Figure 5-3: p++ contact optimization

D. Heatsinking

Additionally, the lasers can be soldered to a heatsink to dissipate heat during testing to achieve CW operation. The heatsink used is Cu and about 1 cm^3 in size. Pd/Sn/Ag solder is used to attach the laser chip to the heatsink.

E. Topside n-contact Process V1

Instead of using a backside n-contact, a topside n-contact can be used. There are several possible benefits to this scheme. A topside n-contact can incorporate a highly doped grown n-contact layer to lower contact resistance. The contact can be annealed to further lower contact resistance. The backside contact requires conduction through the substrate, which could also be a source of additional series resistance. Additionally, the coupled laser mentioned in the previous section requires a topside n-contact so as to not inject through the optically pumped wells.

The topside n-contact epi structure is shown in Figure 5-4. It includes an n-contact layer and a lower doped interlayer to reduce the mode overlap with the higher doped n-contact layer and the optical loss due to absorption.

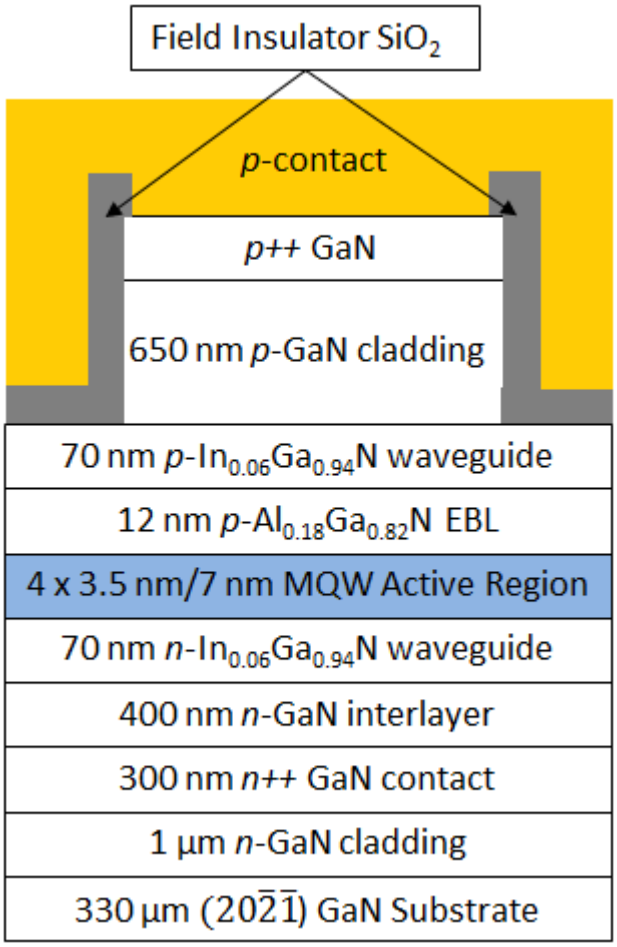
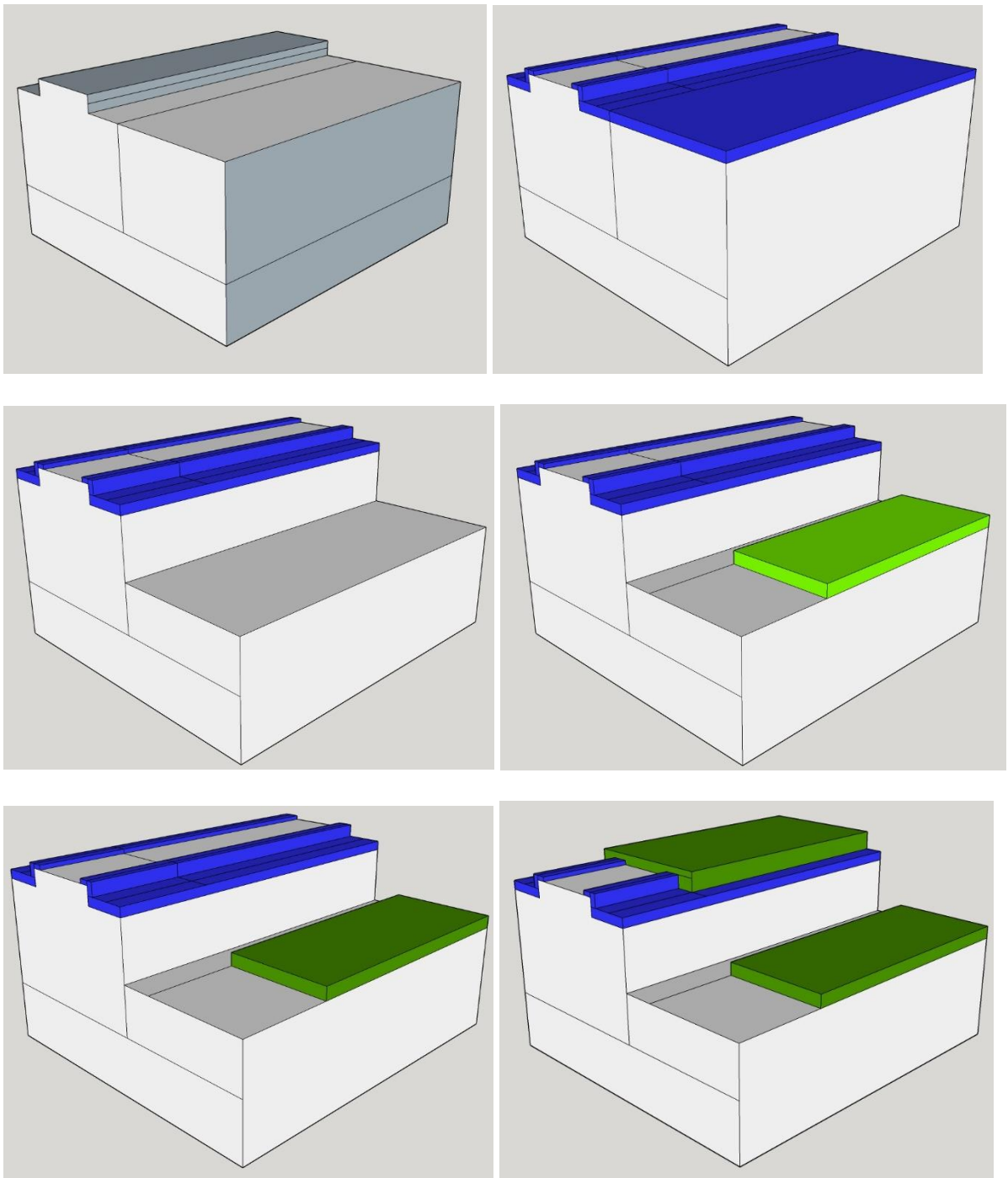
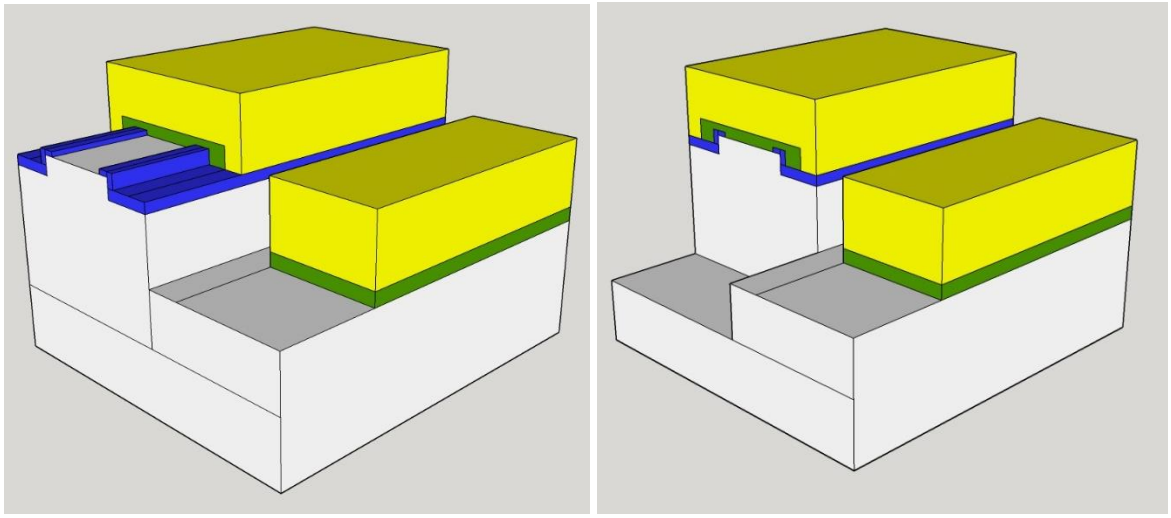


Figure 5-4: Topside n-contact Epitaxial Structure

Figure 5-5 shows the process flow. The process begins with the same ridge etch and self-aligned SiO_2 deposition and liftoff from the other process. Then a trench is etched with RIE down to the n-contact layer. The n contact is deposited Ti/Al/Ni/Au by e-beam deposition, and then the contact is annealed at 550 °C for 3 mins in a rapid thermal annealer (RTA). Then the p-contact of Pd/Au is deposited. p- and n-pads of Ti/Au are deposited in a joint e-beam

deposition step, and then the facet is etched. Step-by-step details of the process are presented in the appendix.





1. Ridge etch
2. Field insulator deposition
3. n-via etch
4. n-contact deposition

5. n-contact anneal
6. p-contact deposition
7. p- and n- pad deposition
8. Facet etch

Figure 5-5: Topside n-contact process steps

F. Topside n-contact Optimization

The growth conditions of the n++ contact layer were explored. Figure 5-6 shows I-V results of n-n measurements for different n++ growth conditions. If the doping was at least 5 x 10^{19} /cm^3, as measured by SIMS, the contact was ohmic. This corresponds with a disilane flow of 10 sccm under growth conditions using TEG at 850 °C. The anneal conditions of 550 °C for 3 mins were adapted from previous work. This is shown via circular TLM measurement in Figure 5-7, with contact resistance of 1 x 10^{-6} (Ω-cm^2). Further optimizations of this process have been done, by Yonkee et al in unpublished work, using an Al contact and vacuum anealing.

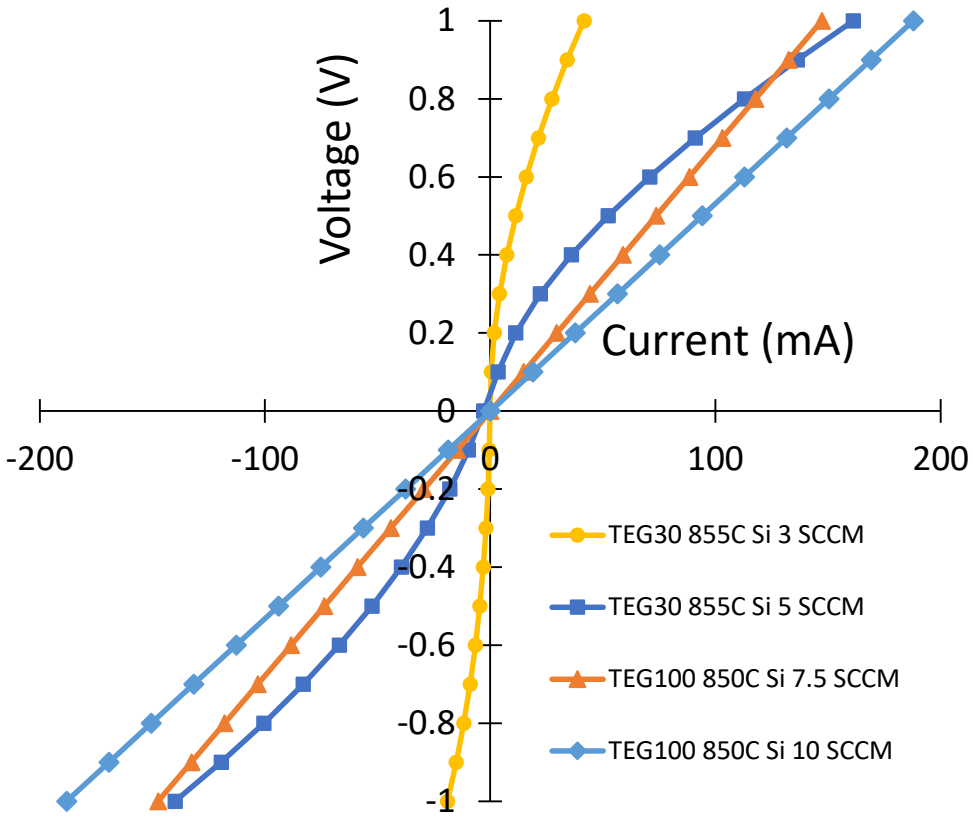
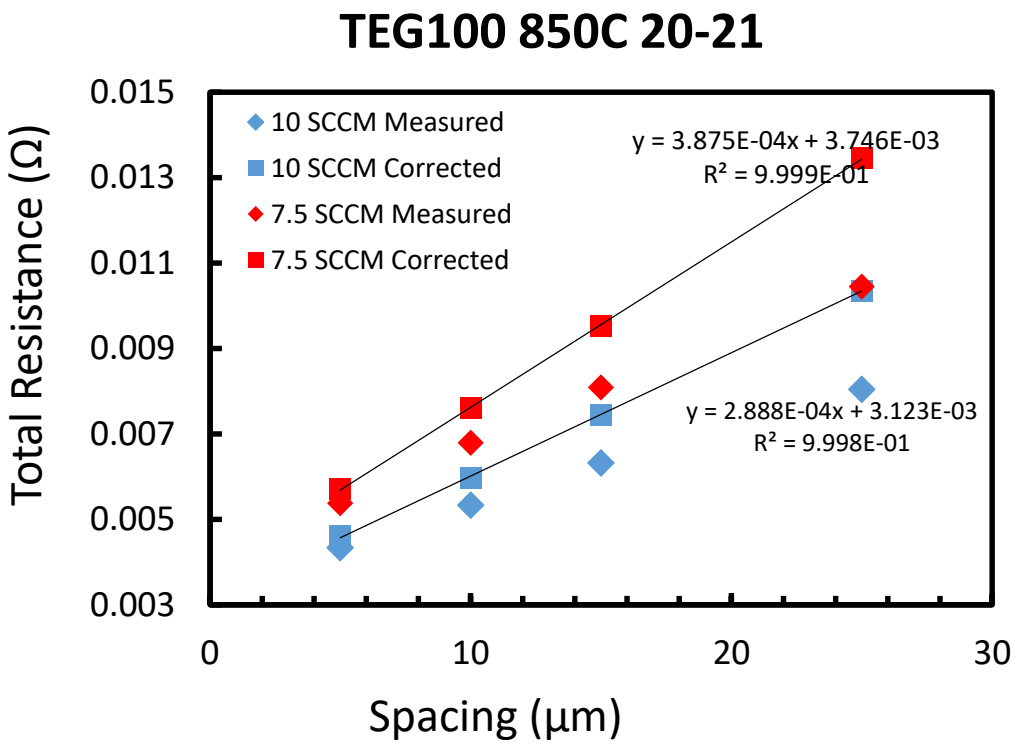


Figure 5-6: n-contact I-V measurement

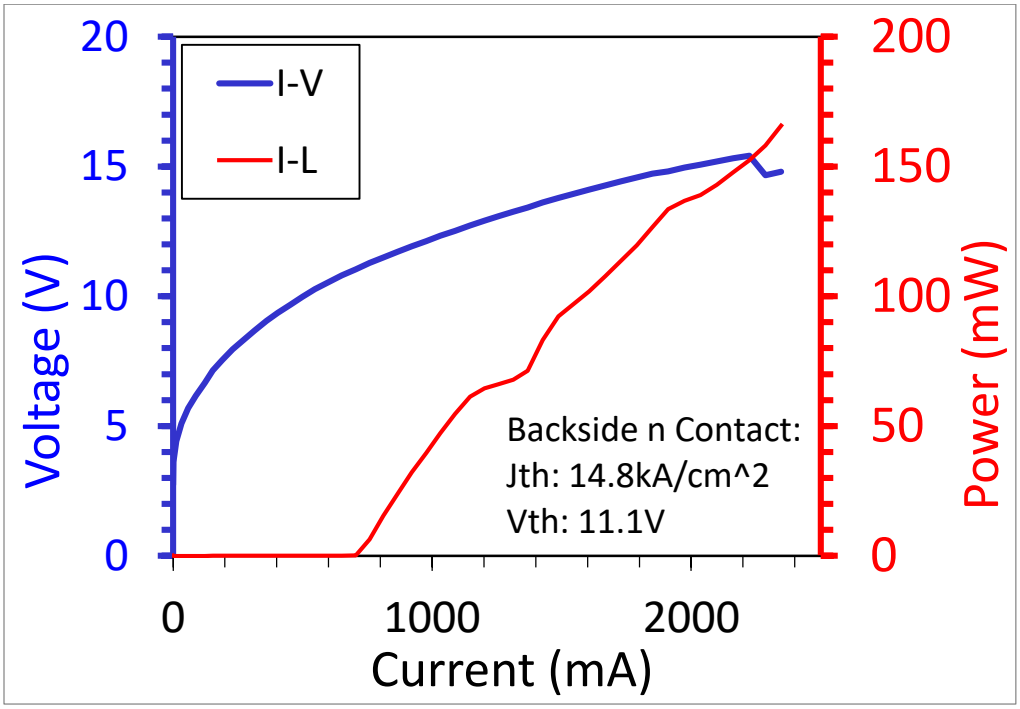


Si_2H_6	7.5 SCCM	10 SCCM
L_T (µm)	5.4082	4.8343
R_{sh} (Ω/□)	3.8954	2.9029
ρ_c (Ω-cm^2)	9.104E-07	8.491E-07

Figure 5-7: n- TLM Measurement

Figure 5-8 shows results of a laser fabricated with both topside and backside n-contacts to compare the performance. Figure 5-9 shows a scatter plot of threshold voltage and threshold current density for these devices. The topside n-contact showed no difference in threshold current density, but ~1.5 V higher threshold voltage, indicating the topside n-contact added no additional optical loss but the electrical performance needed to be further optimized.

Vacuum annealed n-contacts have shown promise; this will also be investigated in the future.



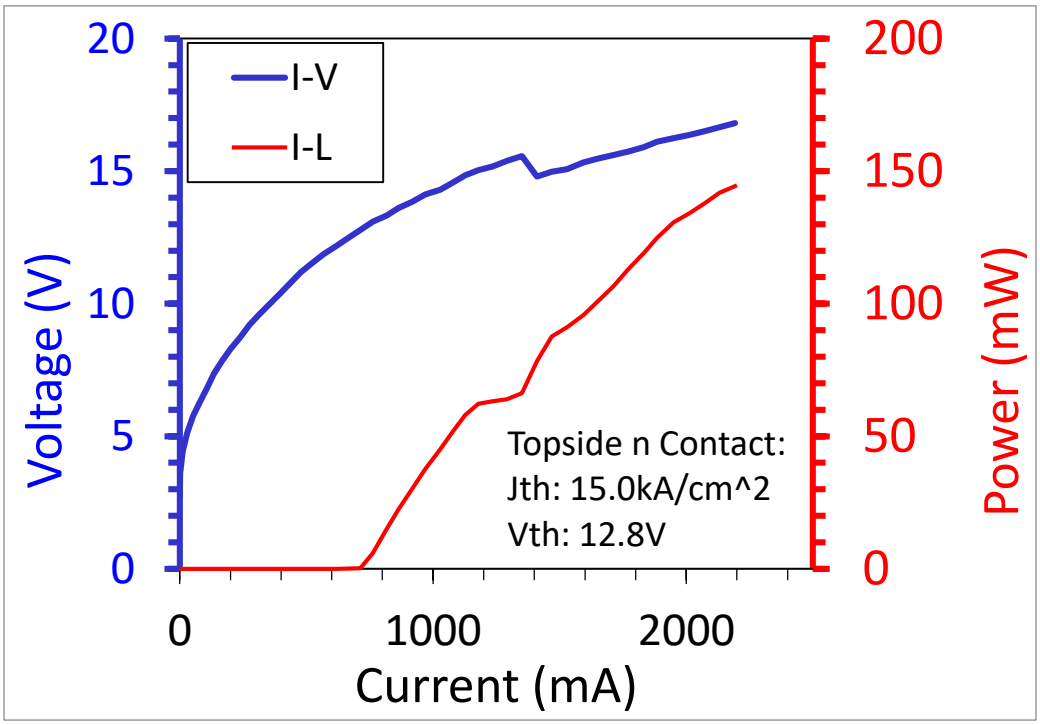


Figure 5-8: L-I-V Curves of Topside n LDs

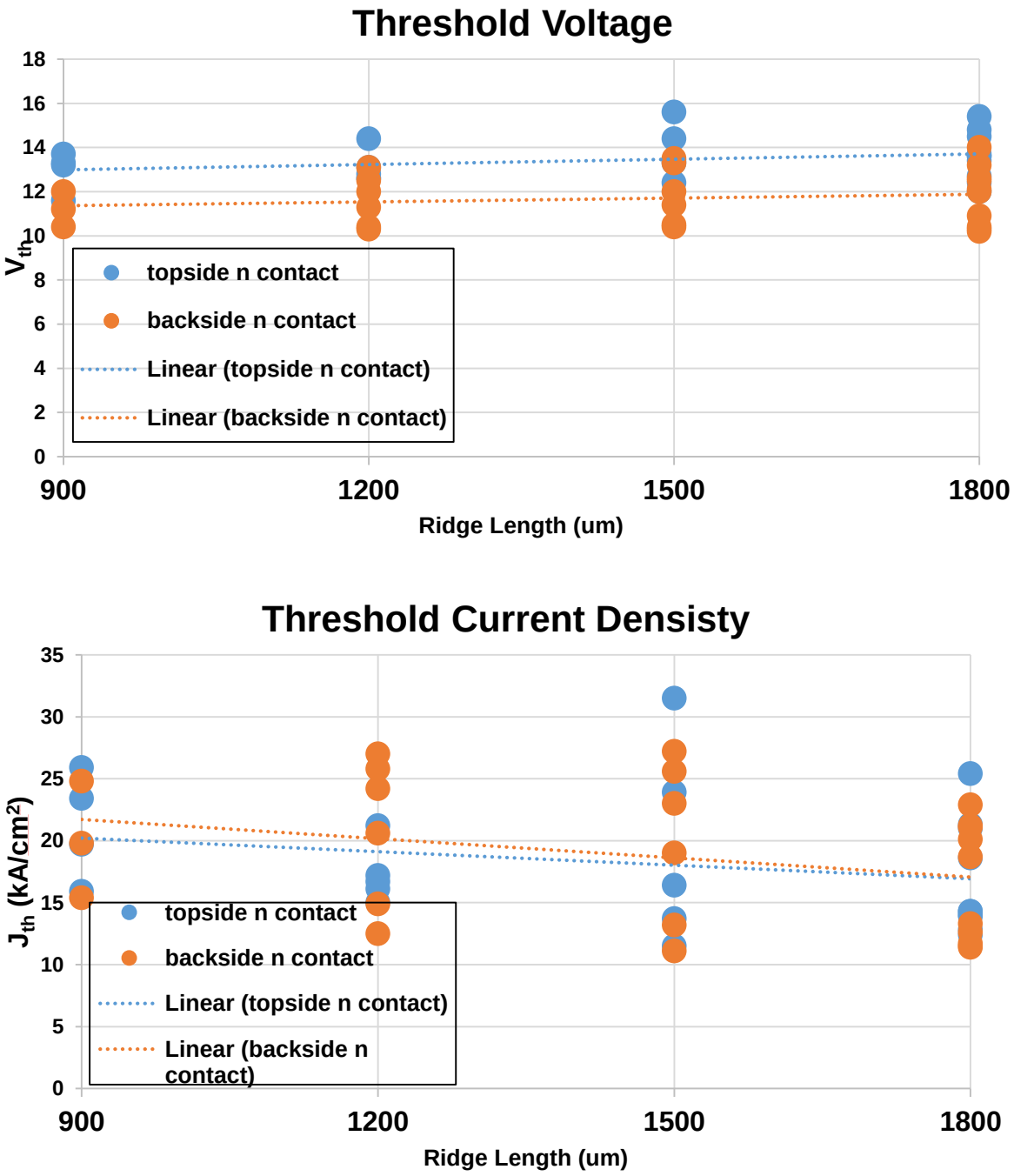


Figure 5-9: Scatter of V_{th} and J_{th} for Topside n-contact LD

G. CAIBE Facet Etching

The mirror facets of LDs are very important, and careful consideration must be given to the process of forming the facets.

1. Introduction

The most common method in other III-V material systems of forming LD mirror facets is cleaving along a crystallographic direction perpendicular to the laser cavity. Semipolar planes however do not have easy access to a perpendicular cleavage plane, since the high gain direction is parallel to the c-axis in the GaN crystal.[6]

Other methods of forming facets are possible. A common method used is reactive ion etching (RIE), but this method has produced unacceptably rough and angled facets, as seen in Figure 5-10.

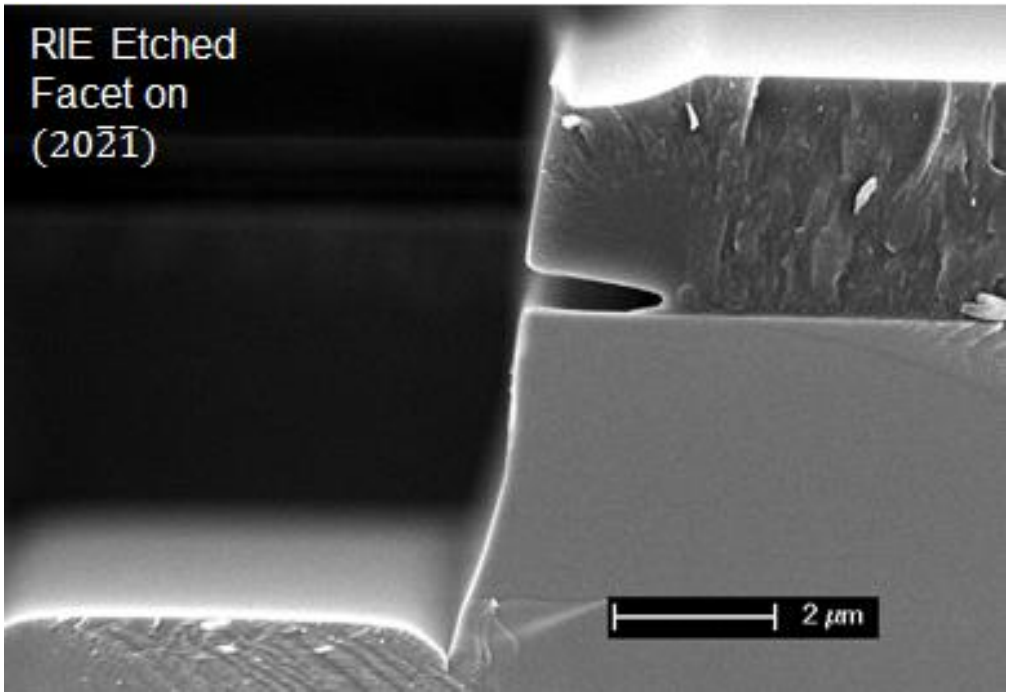


Figure 5-10: Semipolar RIE Etched Facet

The facet is measured to be sloped from vertical approximately 6 degrees. As can be seen in Figure 5-11, this results over 60 % parasitic mirror loss.

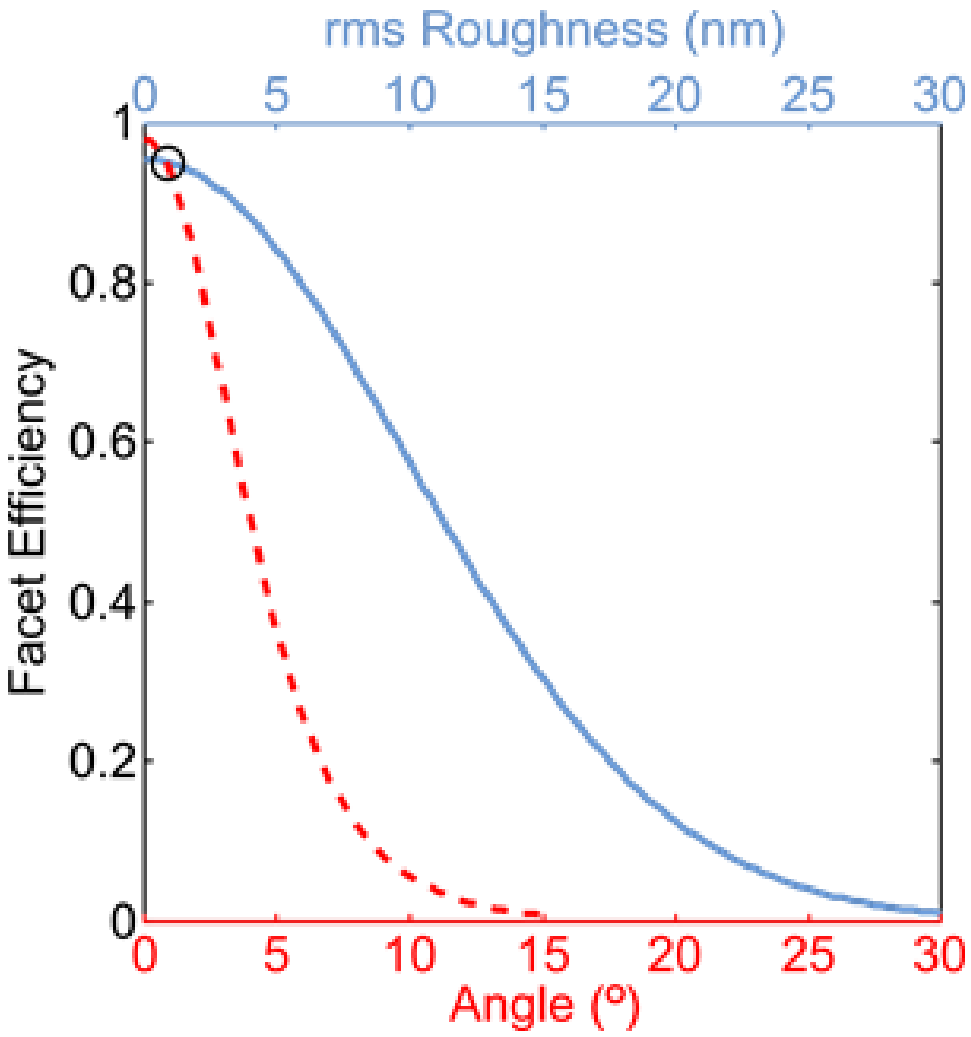


Figure 5-11: Facet Efficiency for Angled and Rough Facets © IOP Publishing. Reproduced with permission. All rights reserved [7]

The circle in this figure represents the final optimized facet etch that will be described in this section. Another process than can be used is facet polishing. This can be used to create smooth and vertical facets, however the process is very time consuming (approximately 4 work-days for 1 sample versus 1 work day for etching). The polishing process also has a steep learning

curve and has many steps which require very careful alignment, something which should not be the case for optimized etching.

Chemically Assisted Ion Beam Etching (CAIBE) has been shown by various groups to produce smooth and vertical facets on c-plane GaN. [8]–[12] Adapting it on semipolar required a total optimization from scratch. This section will discuss that procedure.

2. Overview of CAIBE Tool and Process

The CAIBE process for GaN etching uses an Ar ion beam and Cl_2 ambient gas. A diagram of the process chamber is shown in Figure 5-12. The Ar ion beam is accelerated in a grid setup and is incident upon the sample (blue). The angle of incidence can be tightly controlled by the adjustment of the stage tilt. The Cl_2 gas is injected in a ring around the stage (green). The stage tilt will control the angle of the etch by controlling the angle of the incident ions.

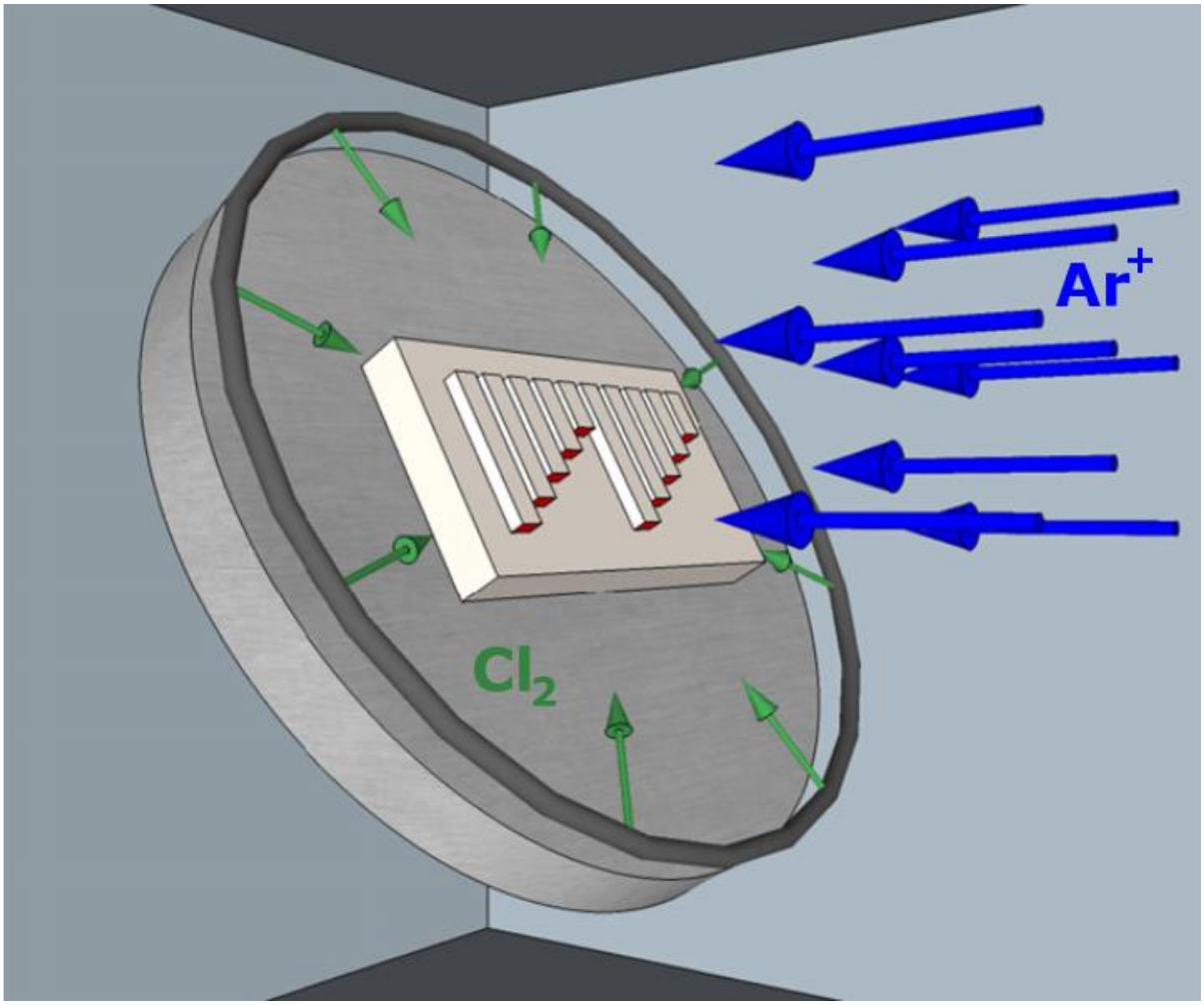


Figure 5-12: Schematic of CAIBE System© IOP Publishing. Reproduced with permission. All rights reserved [7]

The beam parameters such as beam current and voltage can be controlled independently. Beam current adjustments have a linear impact on the etching rate, and is the most straightforward way to control the etch rate. Beam voltage can also impact the etch rate via the energy of the impinging ions. Both of these parameters must be optimized to find an optimal etch rate for a smooth etch as is discussed in the next section. The Cl_2 flow must also be adjusted to control the roughness. The etch rate is also dependent on the tilt, which must also be taken into account when optimizing the roughness.

3. Major Parameters Impacting Etch: Etch Rate, Cl_2 flow and Tilt

The major parameters affecting the etch quality will be discussed in this section. First, if using photoresist (PR), the etch must be periodically interrupted to avoid degradation of the PR. As seen in Figure 5-13, significant PR degradation is seen if etching for more than 5 minutes continuously.

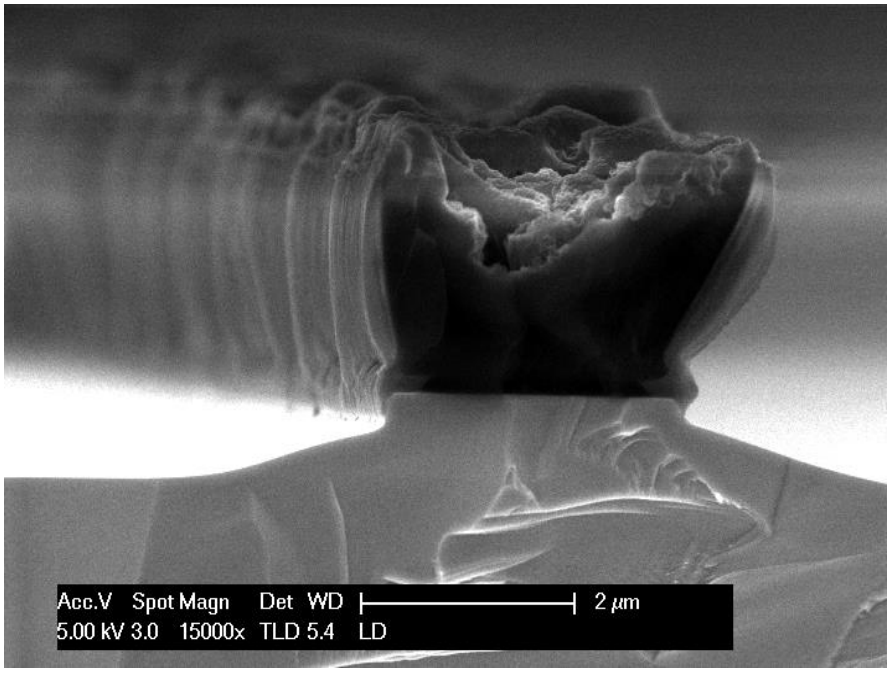


Figure 5-13: Degraded PR

The institution of 5-minute cooling steps after 5 minutes of etching proved to be enough to control this issue, Figure 5-14 shows PR quality after 6 cycles of this procedure of alternating etching and cooling for 30 total minutes of etching. This can be extended to at least 2 hours of etching with thick PR.

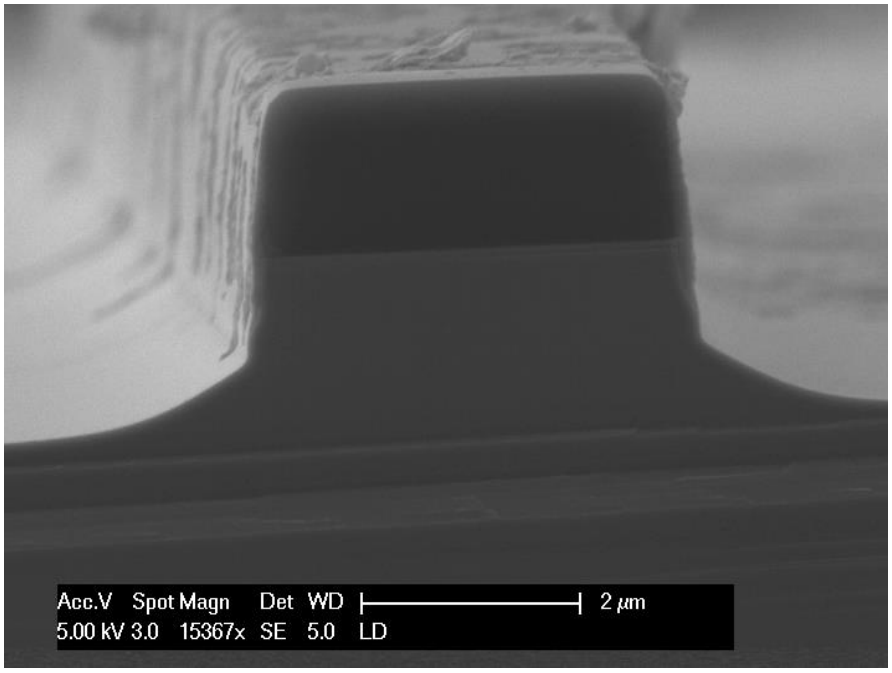


Figure 5-14: PR Integrity Maintained

The effect of Cl_2 flow is illustrated in Figure 5-15. A clear reduction in roughness is seen as the Cl_2 flow is increased to 20 sccm, the maximum flow available in the tool.

The tilt of the stage will determine the etch profile. Figure 5-16 (a)-(c) shows etches where the profile is sloped, undercut, and vertical respectively. The optimized tilt angle may drift over time, at present the optimized tilt angle is -29 degrees.

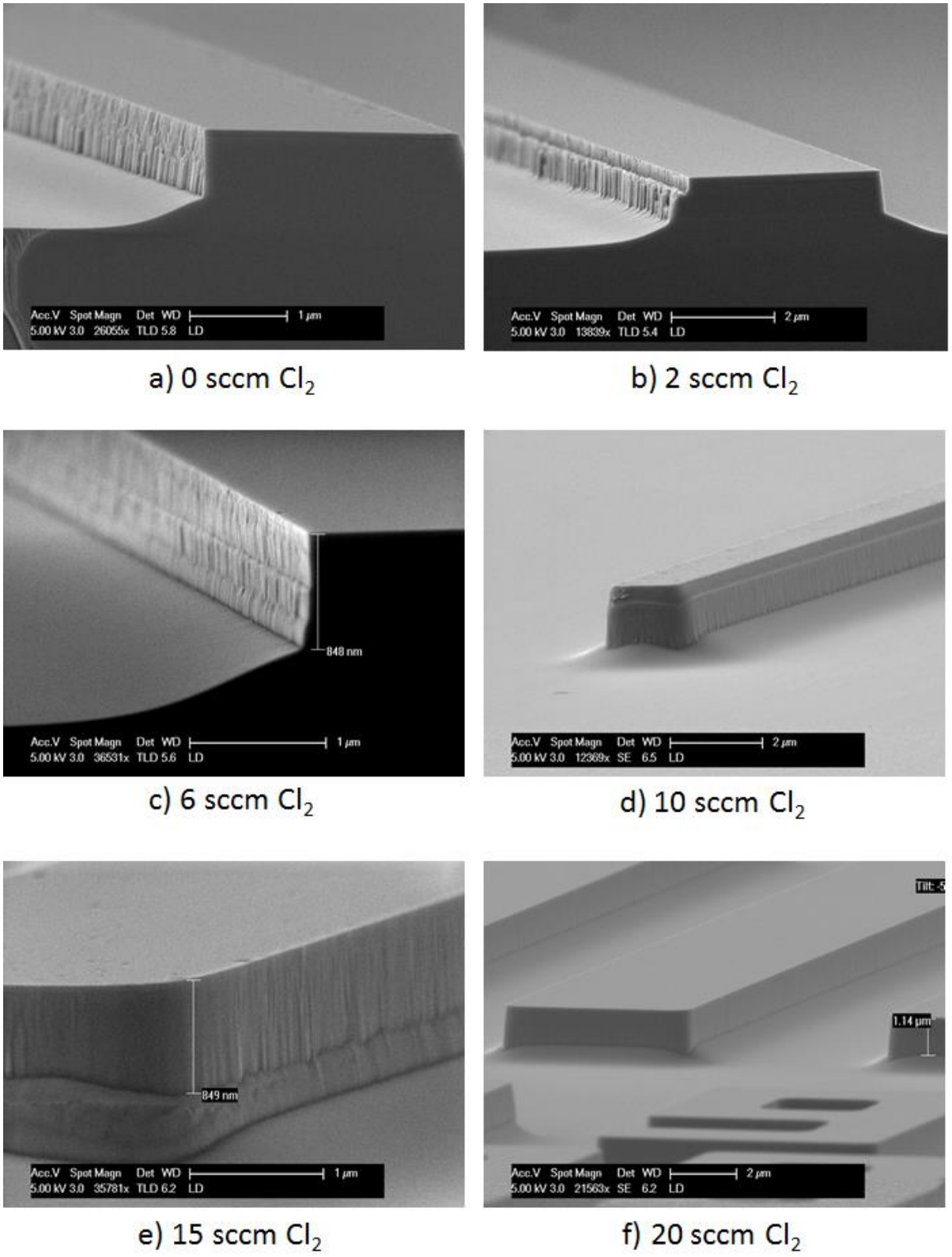


Figure 5-15: Effect of Cl_2 flow on CAIBE Etch Roughness a)-f) 0-20 sccm Cl_2

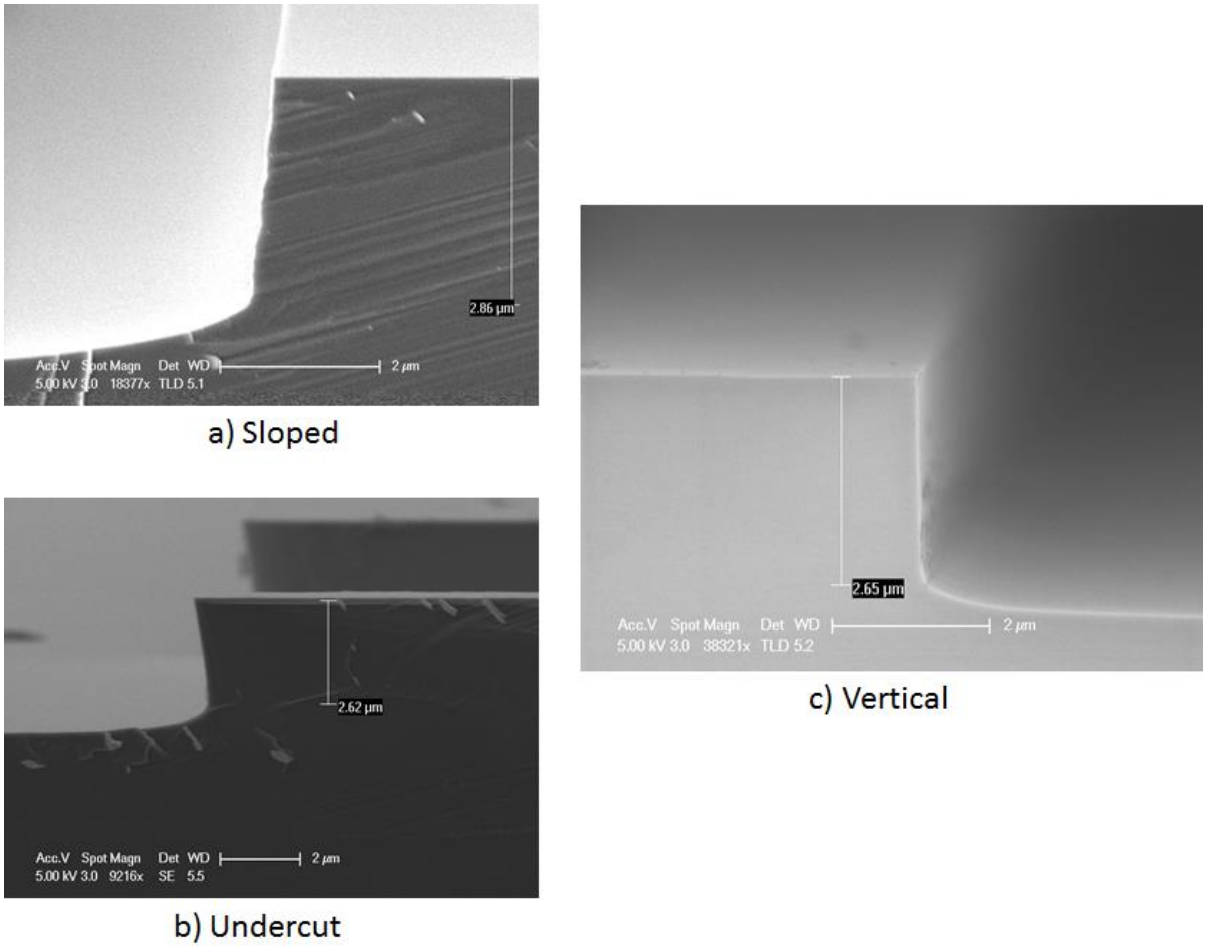


Figure 5-16: Illustration of Etch Profile Tunability

4. Characterization of Final Optimized Etch

In the course of optimizing the etch rate and verticality, it was necessary to not rotate the sample, and etch one facet at a time. This improved etch rate and reduced the "shoe" profile at the bottom of the etch. Figure 5-17 shows the process whereby this is accomplished for front and back facet formation: (a) etch with the front LD facet facing the beam, which shadows the back facet (b) strip and reapply a new shifted PR mask to protect the front facet and reveal a planar surface for the back facet etch, (c) etch the sample with the back LD facet facing the Ar ion beam (d) finished front and back facets, (e) etch profile of a ridge formed on m-plane GaN

by a CAIBE process with rotation (etch rate = 35 nm min−1) (f) etch profile of a ridge formed on m- plane GaN by separately etching the two faces without rotation (etch rate = 63 nm min−1). This etch shows a smaller etch tail, higher facet etch rate, and improved facet verticality.

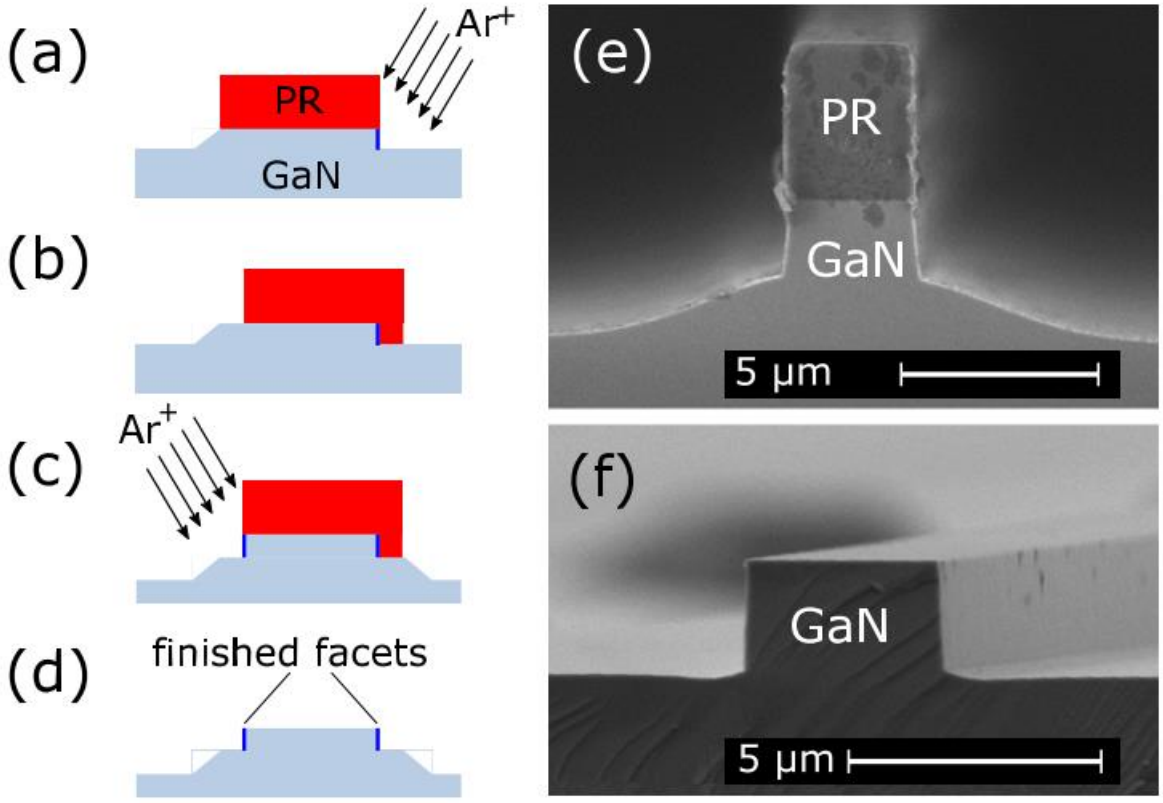


Figure 5-17: Schematic of Final CAIBE Etch Process © IOP Publishing. Reproduced with permission. All rights reserved [7]

The final facet etch profile and roughness are shown in Figure 5-18. An angle of 89 degrees from vertical and a line edge roughness of 2.0 nm as measured by planar image processing. The line edge roughness was used because it was found that any etch roughness is transferred from the PR and transfers through the sample.

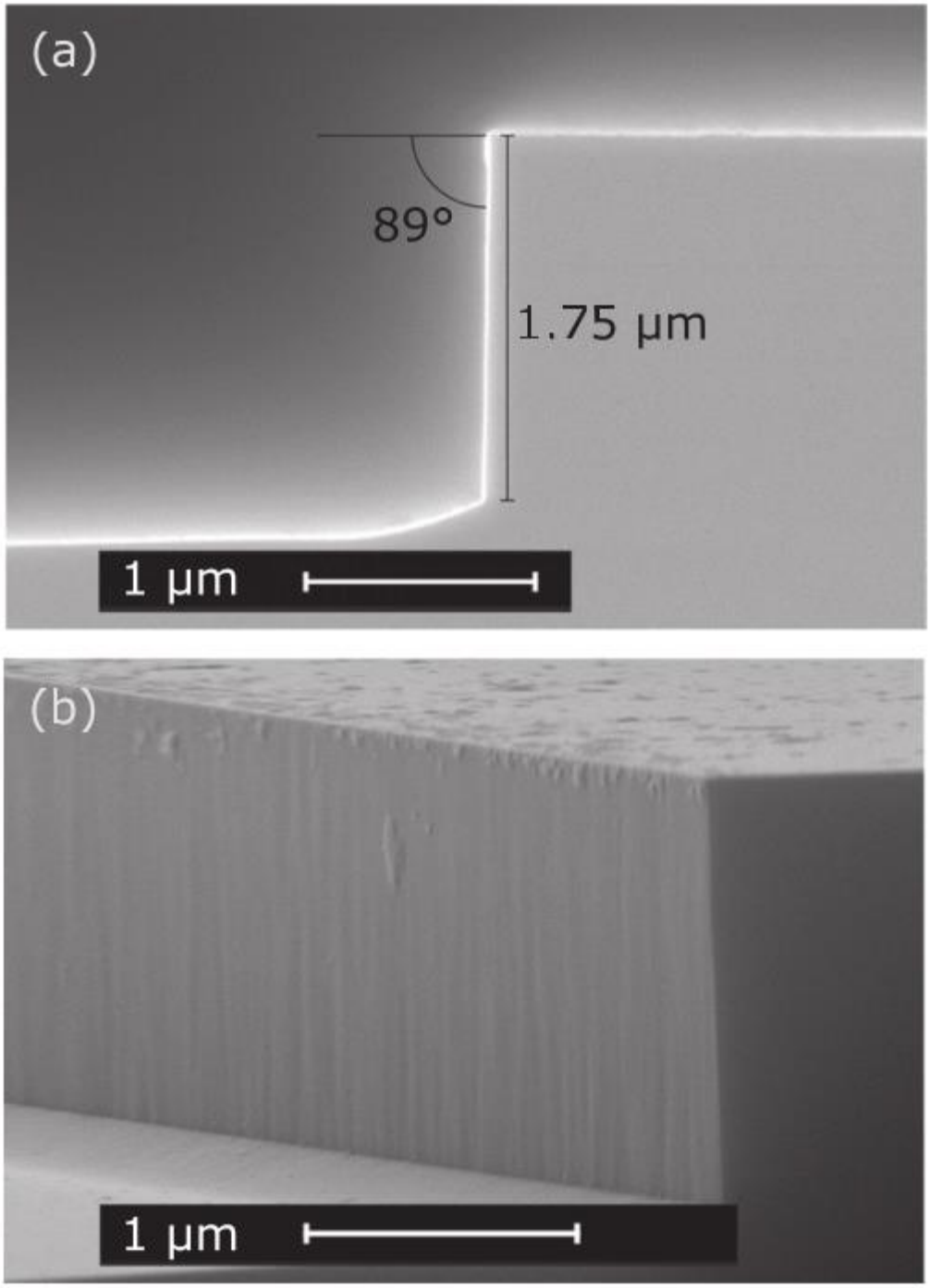


Figure 5-18: Images of Optimized Etch © IOP Publishing. Reproduced with permission. All rights reserved Reproduced with the permission of AIP Publishing. [7]

The LDs made with CAIBE etched facets showed reduced threshold current and a tighter distribution, as can be seen in Figure 5-19.

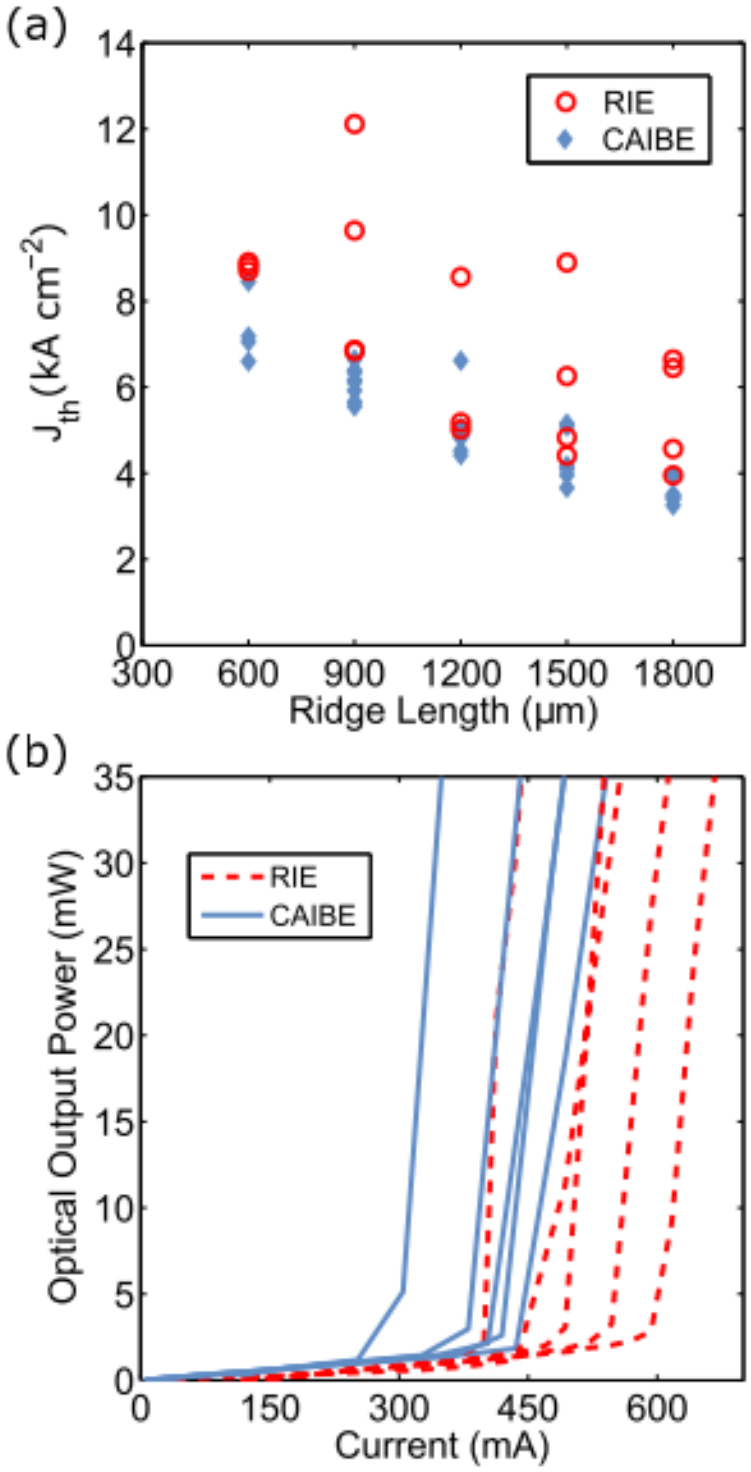


Figure 5-19: Threshold Current for CAIBE and RIE Etched Facet LDs © IOP Publishing. Reproduced with permission. All rights reserved [7]

The optimized etch conditions have the potential to drift over time based on chamber condition and any chamber maintenance that is done, so the etch must be monitored and the tilt and beam current adjusted if necessary.

H. New Etched Facet Mask Layout

The legacy process for etched facets involved interleaved lasers as seen in Figure 5-20. This allowed for many devices per chip but did not allow for singulation or the measurement of light out of the other facet. Issues with deposition of dielectric materials for facet coatings made it important to be able to access both facets to test. So, a new laser mask layout was required. This new layout, shown in Figure 5-21, places similar sized lasers next to one another with an empty space in the middle to allow for dicing and then accessing the inner facet. This could also allow for the removal of potential shadowing issues for facet coating. The process was developed for both topside and backside n-contact use.

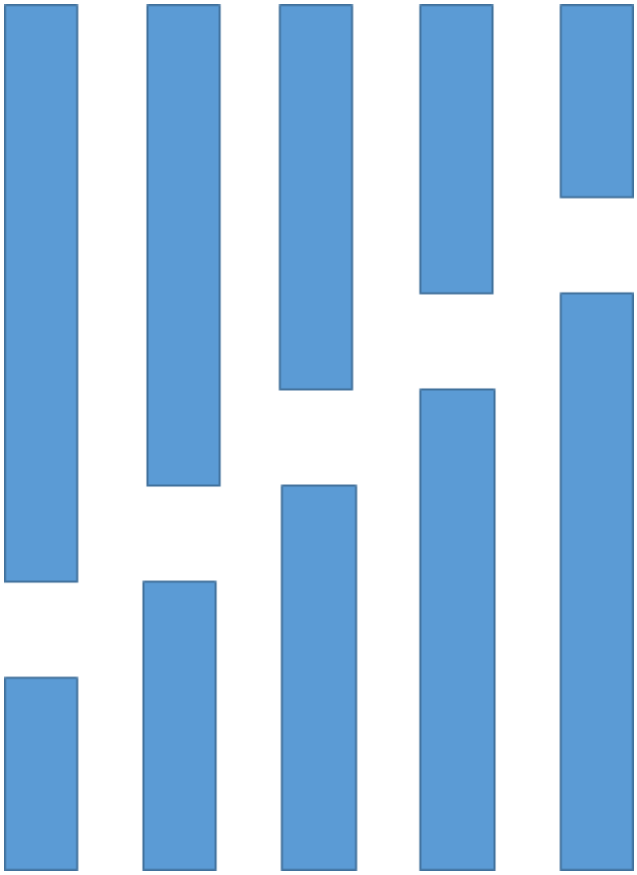


Figure 5-20: Legacy Etched Facet Mask Layout

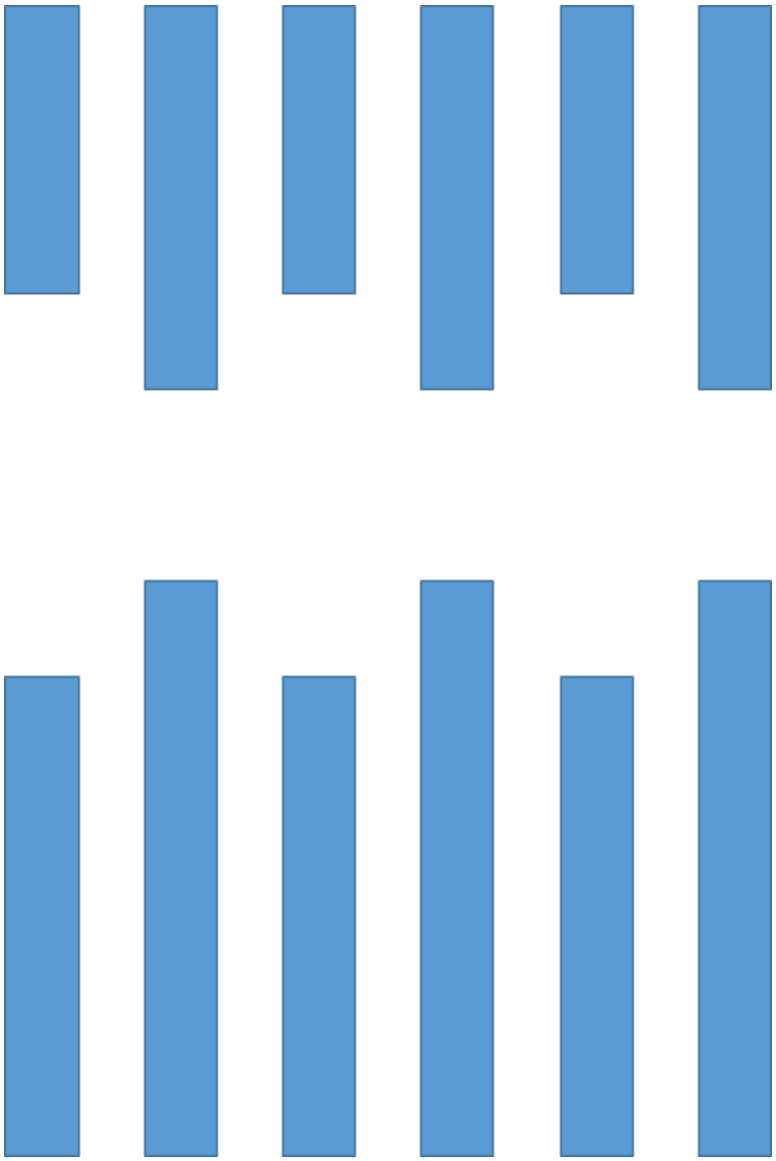


Figure 5-21: New Etched Facet Mask Layout

I. Summary

Many advances in LD fabrication were presented in this chapter. Every part of the process was improved, the ridge etching, p and n contact deposition, and facet formation. Topside n and improved p contacts were demonstrated. More research into low resistance contacts and facet coatings is needed.

J. References

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6. LD Results I: Measurements of Internal Loss and Injection Efficiency

A. Introduction

Since the first demonstration of III-nitride laser diodes (LDs) in the 1990s,[1] these devices have found applications in optical storage, projection displays, and other areas. Future applications may include visible light communication[2] and laser-based white lighting.[3]–[6] As mentioned previously, for lighting applications LDs have advantages over LEDs including higher power per chip area and the absence of efficiency droop above threshold. Most commercial III-nitride LDs are grown on the basal *c*-plane of GaN, either on foreign substrates or on bulk GaN substrates.[7] LDs grown on nonpolar or semipolar planes have several key advantages, including higher wavefunction overlap due to eliminated or reduced polarization fields,[8] higher gain,[9], [10] and reduced wavelength shift with increasing current density.[11], [12] The $(20\bar{2}\bar{1})$ plane has been used to demonstrate high power pulsed[4], [13] and lower power continuous wave (CW)[14] blue LDs.

Despite the clear advantages demonstrated by the $(20\bar{2}\bar{1})$ plane, facet fabrication is difficult because no vertical cleavage plane exists for laser ridges aligned parallel to the high-gain $[11\bar{2}\bar{3}]$ direction. Vertical, smooth, and uniform facets with high device yield are required for good LD performance and industrial implementation, as well as the measurement of internal loss and injection efficiency. These values can be determined by measuring a set of LDs with different cavity lengths according to the cavity length dependent method.[15]

Uniform and near-perfect facets are required for this calculation because a facet power reflectivity (*R)* must be assumed to calculate the mirror loss. From a plot of 1/differential efficiency (η_d) vs. cavity length (L), it is possible to extract the injection efficiency, η_i, from the y-intercept and the internal loss, $\langle \alpha_i \rangle$, from the slope according to Eq. 6-1:

$$\frac{1}{\eta_d} = \frac{\langle \alpha_i \rangle}{\eta_i ln(1/R)} L + \frac{1}{\eta_i} \tag{6-1}$$

Farrell *et al.* previously used this method for *m*-plane violet LDs to report an internal loss of 9.8 cm^{-1} and an injection efficiency of 66%.[16] Other groups report internal losses near this value for *c*-plane LDs.[17], [18] Several groups have also used the Hakki-Paoli method to extract loss for LDs grown on various planes of GaN.[10], [19], [20]

Since semipolar LDs lack a vertical cleavage plane for the formation of cleaved facets, alternative dry etching or mechanical polishing processes must be used to form facets. Previously, demonstrations of etched facets on semipolar and nonpolar planes have used reactive ion etching (RIE) or inductively coupled plasma (ICP) etching.[13], [14], [21], [22] It has been shown that these facet etch methods can introduce parasitic losses due to etch roughness and/or facet inclination, which may be different on different planes and vary across a wafer.[22] Using a focused ion beam (FIB), smooth vertical facets can be realized but this process is time-consuming.[14], [22] Dicing and then using a physical polishing process to form the facets can eliminate some of these issues,[4], [23] but it is also very time consuming and there are issues with reproducibility, as discussed previously in this dissertation.

In contrast, chemically assisted ion beam etching (CAIBE) is a technique which has shown vertical and smooth facets on *c*-plane GaN. Various groups reported facet angles within 2° of vertical with root mean square (rms) roughnesses of 4 nm - 7 nm in the 1990s.[24]–[27] Recently, the CAIBE technique has been applied to nonpolar and semipolar planes to produce

etches with rms line edge roughness of 2.0 nm and angle 1° from vertical.[28] Figure 6-1 shows scanning electron microscope (SEM) images of a CAIBE etch.

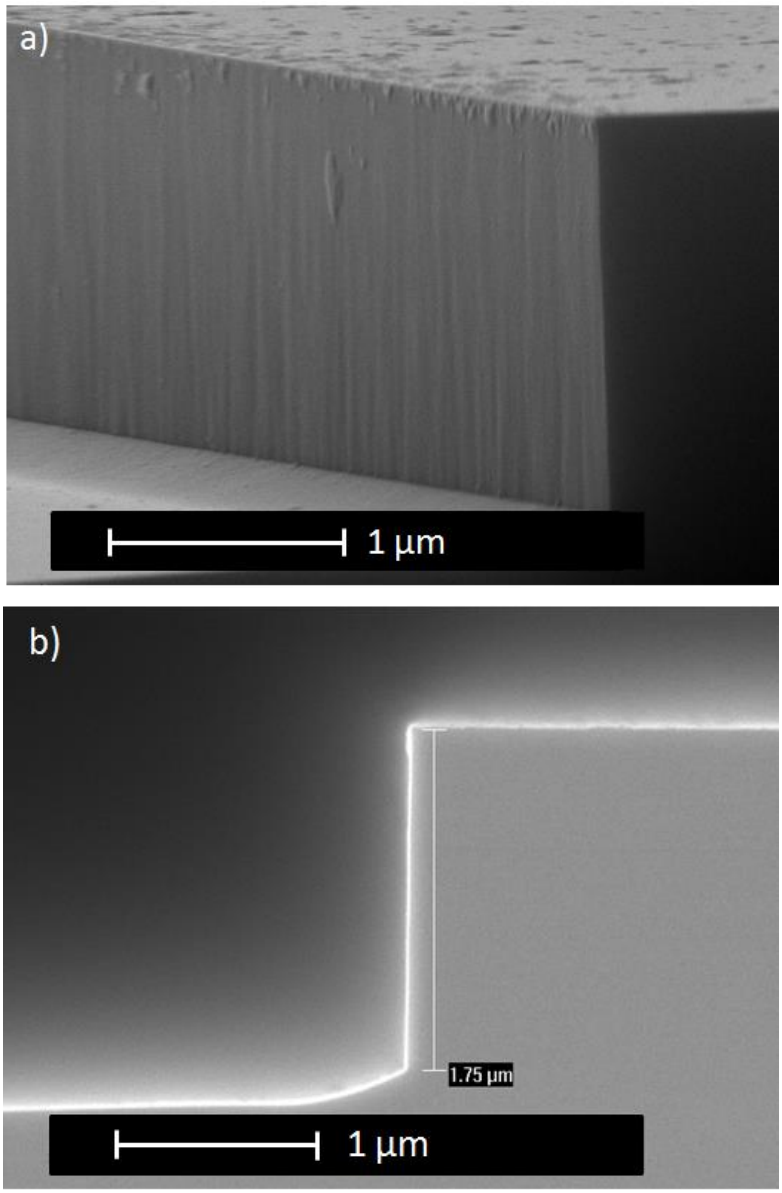

Figure 6-1 a) SEM of a typical CAIBE etch b) Cross-sectional SEM of a CAIBE etch showing the facet verticality. Reproduced with the permission of AIP Publishing.[29]

In this chapter, results of CW blue LDs fabricated with optimized CAIBE etched facets are presented. Internal loss and injection efficiency for these lasers was determined via the cavity length dependent method.

B. Experimental

LDs were grown on free standing bulk $(20\bar{2}\bar{1})$ GaN substrates. The main features of the epitaxial structure are shown in Figure 6-2 and described in detail elsewhere [4] and in previous chapters.

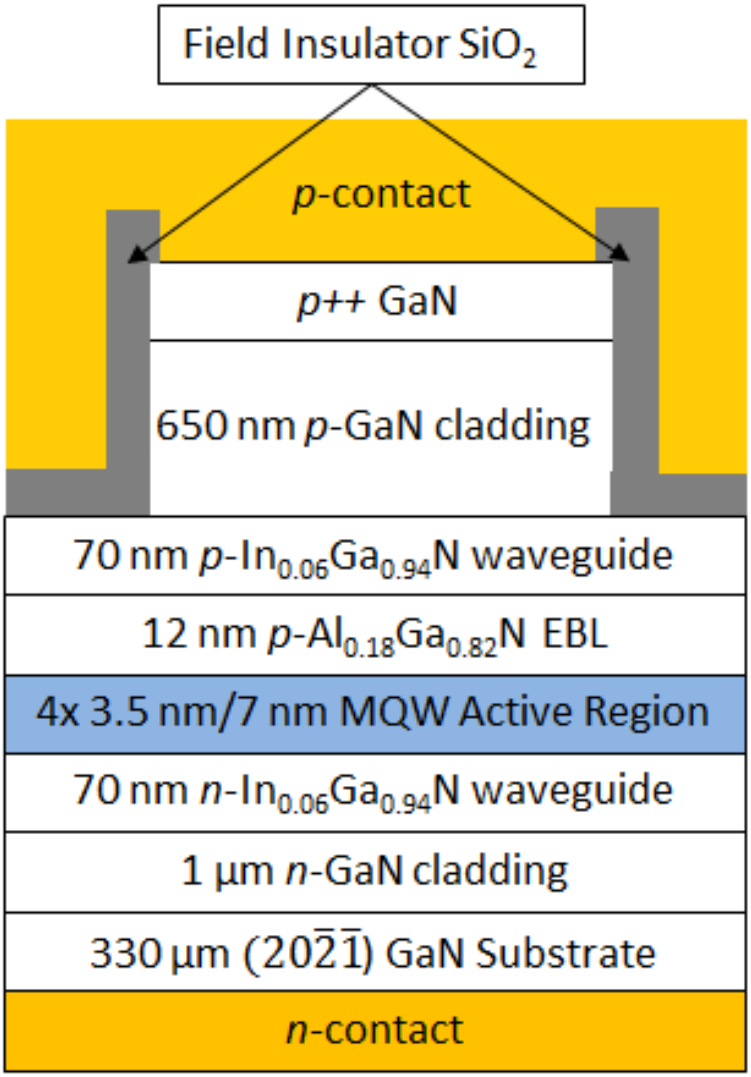

Figure 6-2: Cross-sectional schematic of the LD structure Reproduced with the permission of AIP Publishing.[29]

The epitaxial structure consisted of a 1-µm *n*-GaN cladding, followed by a 10-nm linear composition grade from *n*-GaN to *n*-$In_{0.06}Ga_{0.94}N$, a 50-nm *n*-$In_{0.06}Ga_{0.94}N$ waveguiding layer, and another 10-nm linear grade back down to the first GaN barrier. The active region consisted of an undoped 4-period InGaN/GaN (3.5 nm / 7 nm) multiple quantum well (MQW) emitting at 439 nm followed by a 12-nm *p*-$Al_{0.18}Ga_{0.82}N$ electron blocking layer, which was then linearly graded in composition over 10 nm to *p*-GaN. The *p*-type waveguiding layer followed

with the same composition grading and thicknesses as in the *n*-type waveguiding layer. The *p*-GaN cladding was 650 nm thick and capped with a *p*++ contact layer. Doping values are given in Table 6-1; these values were measured using secondary ion mass spectroscopy (SIMS).

Laser ridges were formed by RIE and isolated with a SiO_2 field oxide which was lifted off from the ridge using a self-aligned process.[30] Pd/Au *p*-contacts and Ti/Au pads were deposited by electron beam evaporation and liftoff. Facets were formed by CAIBE in an Oxford Ion Mill (Oxford Instruments PlasmaLab 300 IBE/RIBE/CAIBE system) with an Ar ion beam and Cl_2 gas injected in a ring around the sample, with the SiO_2 above the facet removed prior to the CAIBE etch with a wet etch in buffered HF. Al/Ni/Au *n*-contacts were blanket-deposited by e-beam evaporation on the backside of the sample. The samples were soldered with Pd/Sn/Ag solder to a ~2 cm^3 Cu heat sink for CW testing. The cavity lengths of the devices ranged from 900 μm to 1800 μm and the ridge widths ranged from 3 μm to 7.5 μm.

C. Results

All devices lased under pulsed operation at room temperature, confirming the high yield of the CAIBE process. The light-current-voltage (*L*-*I*-*V*) curve for an 1800 μm x 4 μm LD with CAIBE facets and a lasing wavelength of 439 nm is shown in Figure 6-3. The threshold current density (J_{th}) and threshold voltage (V_{th}) of this device were 3.4 kA/cm^2 and 6.5 V, respectively, under pulsed operation with a pulse width of 600 ns and frequency of 10 kHz (0.6 % duty cycle). The lasers were tested under pulsed operation to limit the impact of heating on the measured internal loss and injection efficiency, since heating under CW operation is known to directly impact injection efficiency through heterobarrier leakage and

carrier redistribution in an MQW active region.[31] A η_d of 20% was measured from a single uncoated facet. Pulsed measurements were done using a 2-point probe setup because a 4-point probe setup was not available for pulsed testing. This led to higher measured voltages for pulsed versus CW testing due to the resistance of the probes. The device was also tested under a CW 4-point probe condition with a sweep of several seconds. The voltage in the CW measurement decreased by approximately 1 V (V_{th} decreased from 6.5 to 5.5 V) due to the use of a 4-point probe measurement, which measures and subtracts the voltage drop at the probes. The CW measurement showed an increased J_{th} of 3.8 kA/cm^2 and lower single facet η_d of 14% due to heating. Further optimization of the heat sink and epitaxial design to reduce the device voltage and heating should improve the CW performance.

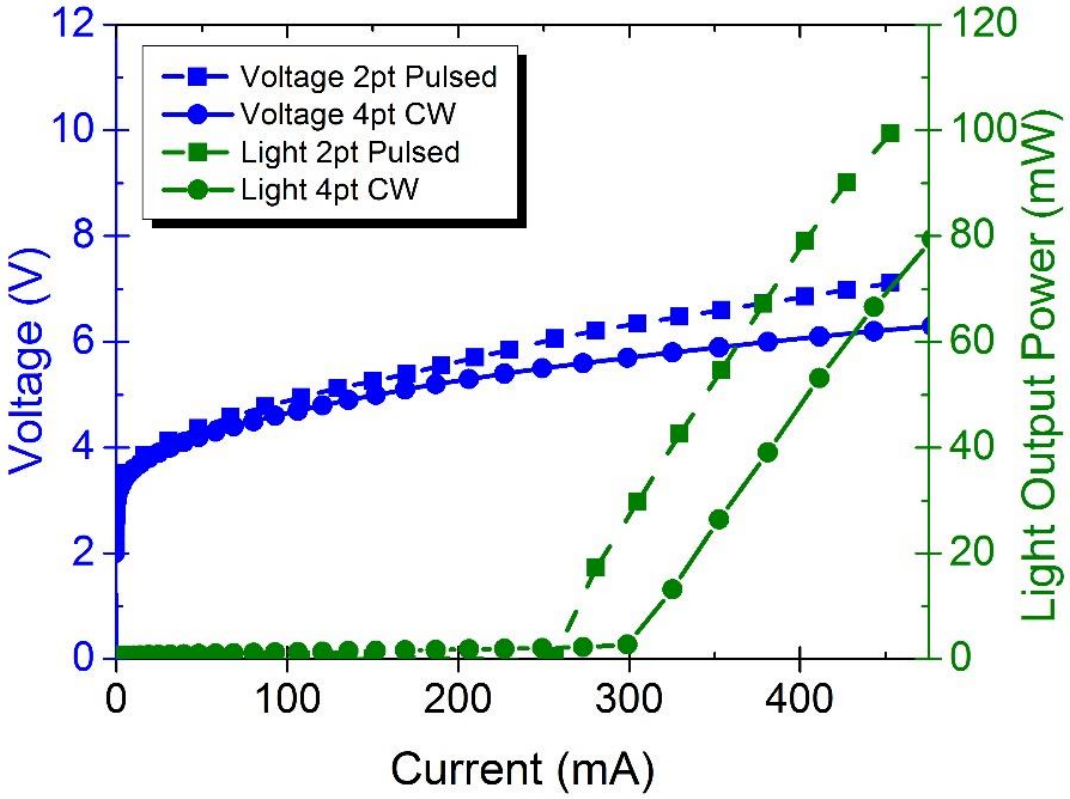

Figure 6-3: Single facet pulsed and CW L-I-V for an 1800 µm × 4 µm LD emitting at 439 nm with uncoated facets. Reproduced with the permission of AIP Publishing.[29]

Figure 6-4 shows the lasing spectrum and far field image for this device. The linewidth of the lasing spectrum was limited by the resolution of the spectrometer, which is approximately 2 nm. In the far field pattern, the lobes above the main pattern are reflections off of the surface of the substrate in front of the facet.

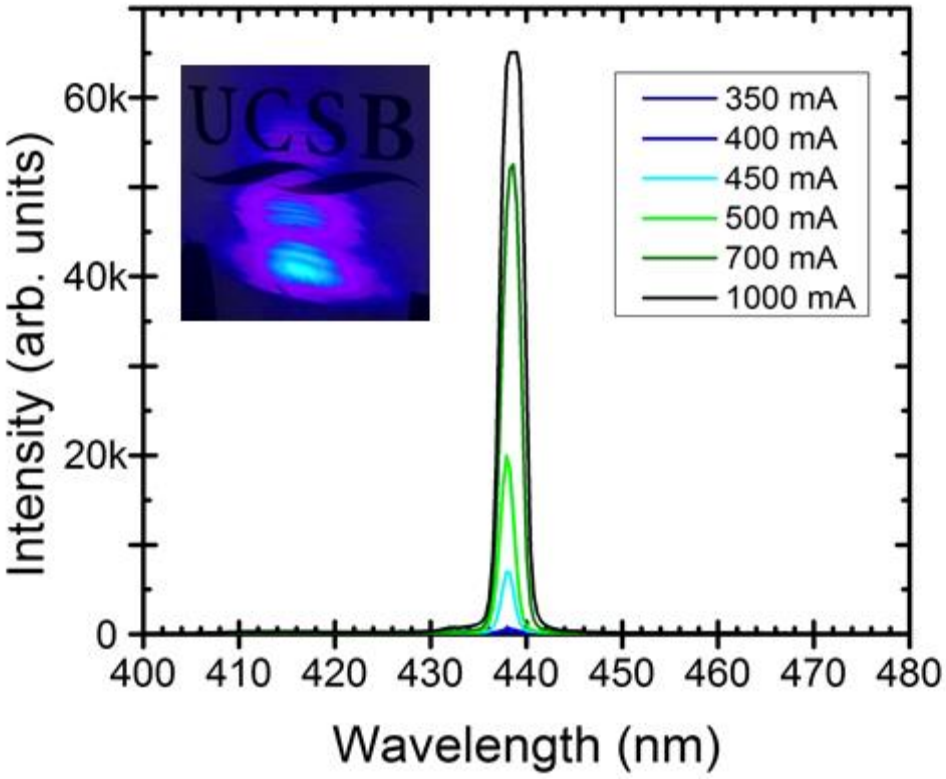

Figure 6-4: Lasing spectrum and far field pattern for a LD with uncoated facets. Reproduced with the permission of AIP Publishing.[29]

D. Analysis and Discussion

Devices with a ridge width of 3 μm and varying lengths from 900 μm to 1800 μm were used for measuring the internal loss and injection efficiency. The measurements were conducted under pulsed operation to minimize the effects of heating. As expected, J_{th} and η_d decreased with increasing laser cavity length. A scatter plot of J_{th} versus cavity length is shown in Figure 6-5.

The lowest J_{th} for this width was 4.2 kA/cm^2 (1800 μm cavity length) and the highest η_d that was measured from one uncoated facet was 30% (900 μm cavity length), indicating the

high quality of the mirror facets formed by CAIBE etching. This is comparable to the best numbers reported for blue nitride LDs.[7], [13] The mask layout allows for measurement out of only one facet, so for the analysis it was assumed that equal power was emitted from both facets. Thus, the differential efficiencies measured from a single facet were doubled for the purposes of the analysis. Figure 6-6 shows a scatter plot of $1/\eta_d$ vs. cavity length. Based on the quality of the facet etches observed, an ideal GaN-air interface (n_{GaN} = 2.54, n_{air} = 1) is assumed, with R = 0.18. The facets were intentionally left uncoated so as to not introduce uncertainty in the calculation of R and mirror loss. Values of internal loss and injection efficiency were obtained from a linear fit to the full set of data. An injection efficiency of 73% and an internal loss of 9 cm^{-1} were obtained.

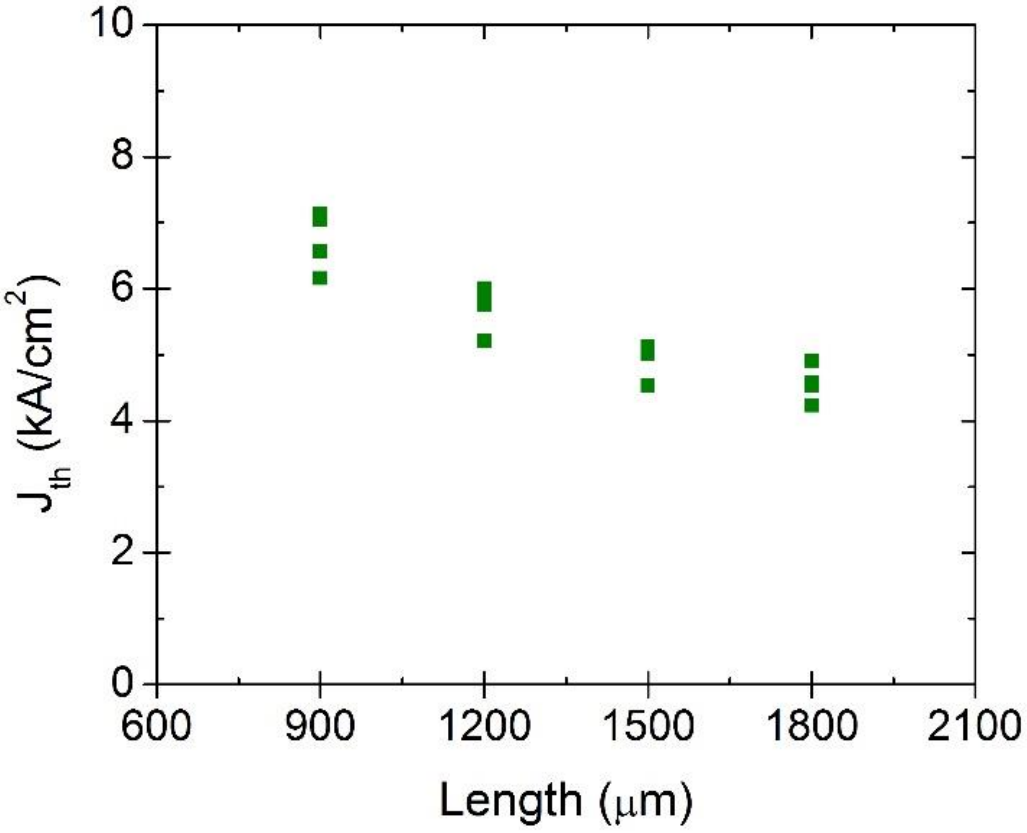

Figure 6-5: Scatter plot of Jth versus cavity length for 3 μm wide LDs. Reproduced with the permission of AIP Publishing.[29]

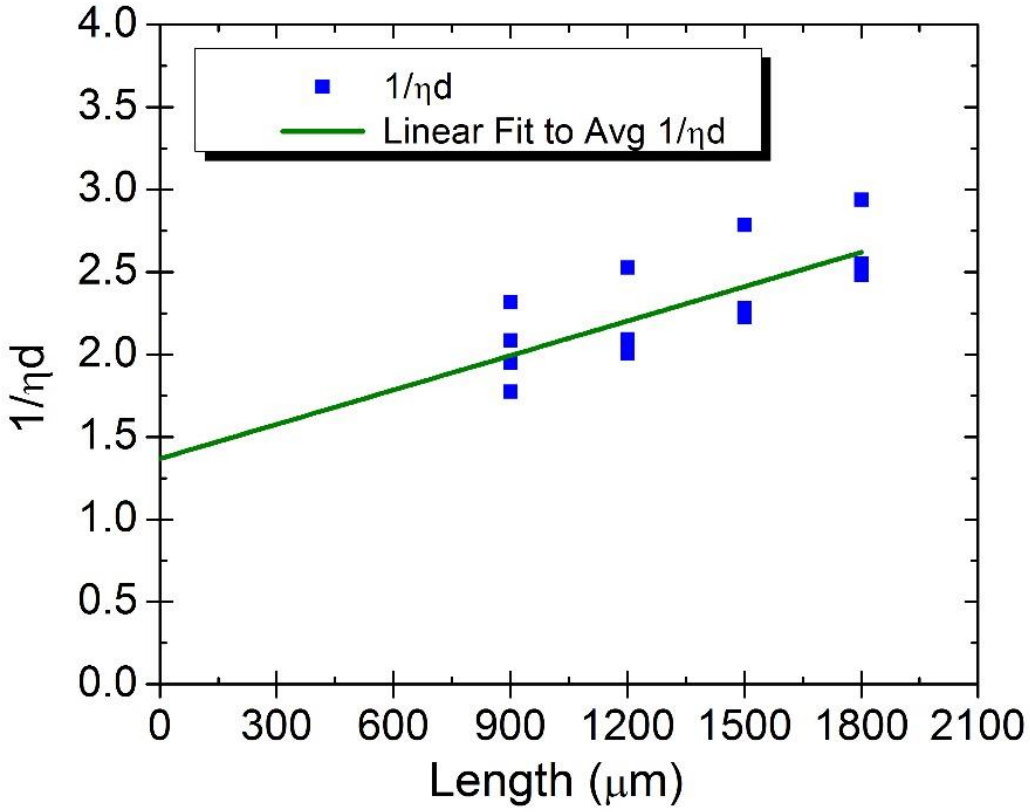

Figure 6-6: 1/ηd versus cavity length for the LDs presented in Fig. 5 with a linear fit to Eq. (6-1). Reproduced with the permission of AIP Publishing. [29]

The transfer matrix method[32] was used to model the 1D mode of the vertical waveguide structure and calculate the confinement factor and internal loss contribution of each layer for these LDs for comparison with the experimental results. The optical mode profile and layer confinement factors and loss were calculated using inputs from the following references: the bowing parameter of the bandgap from Sakalauskas *et al*.,[33] the refractive indices of GaN and AlGaN from Sanford *et al*., [34] and the refractive indices of InGaN from Bergmann *et al*.[35] The modal absorption in each layer was calculated from adapted values from Kioupakis *et al*.[36] A carrier density in the quantum wells of 1×10^{19} cm^{-3} was assumed,

which was adapted from several published estimates.[10], [16] Figure 6-7 shows a plot of refractive index versus depth, a simulated mode profile (black dashed line), and the calculated modal absorption in each layer. The effective index of the mode is also indicated (horizontal dotted line). The calculated QW confinement factor was 0.03 and the calculated internal loss was 9.5 cm^{-1}, which showed good agreement with the experimental results. Table 6-1 provides a list of the losses in each of the major layers and subsections of the structure.

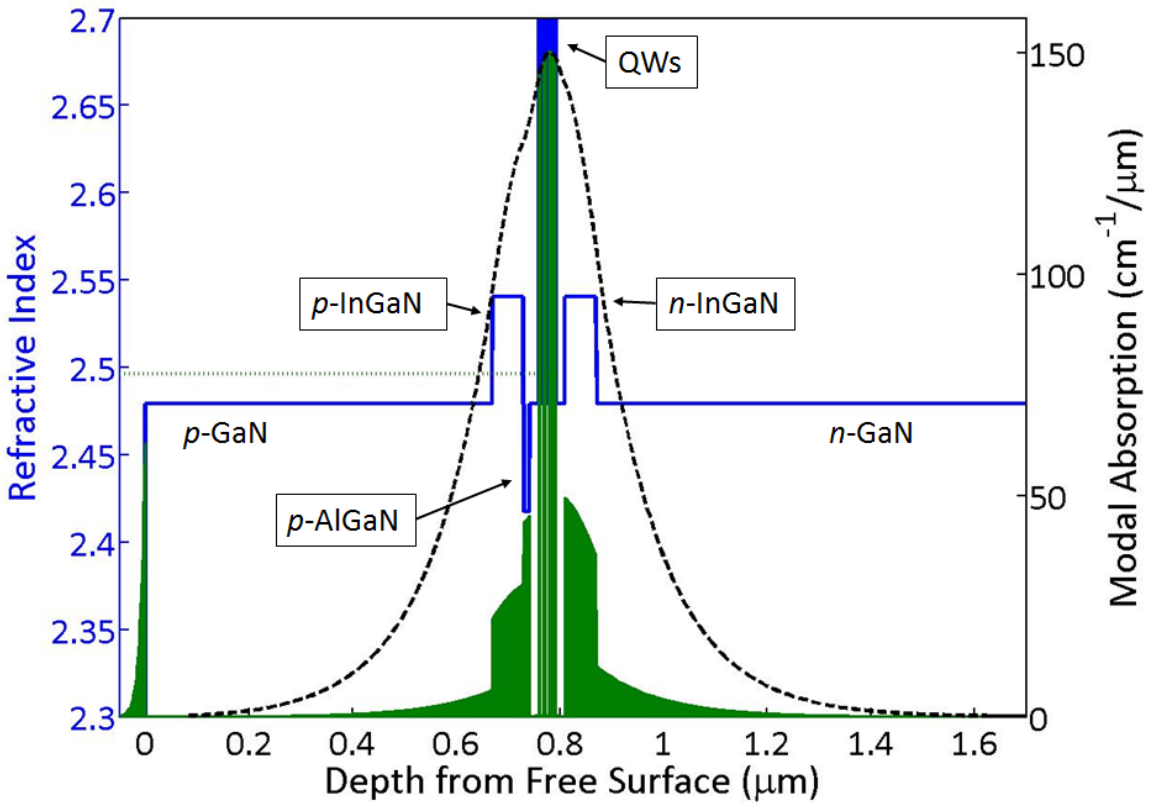

Figure 6-7: Plot of calculated refractive index profile (blue line), mode profile (black dashed line), and modal absorption (green shaded area) as a function of vertical depth from the epitaxial growth surface. Reproduced with the permission of AIP Publishing.[29]

Table 6-1: Materials values used in the model and their calculated contributions to the total loss.

Layer	Material	Doping (measured by SIMS)	Calculated loss (cm^{-1})	Percentage of total loss
p-contact	Pd	-	0.59	6%
p-cladding	GaN	1.7×10^{18} cm^{-3}	0.72	8%
p-waveguide	InGaN	5×10^{18} cm^{-3}	1.6	17%
p-EBL	AlGaN	1×10^{19} cm^{-3}	0.53	6%
	Subtotal p layers		**3.4**	**36%**
MQW	InGaN	-	2.0	20%
	Subtotal active region		**2.0**	**21%**
n-waveguide	InGaN	1×10^{19} cm^{-3}	2.7	28%
n-cladding	GaN	4×10^{18} cm^{-3}	1.4	15%
	Subtotal n layers		**4.1**	**43%**

Total	**9.5**	**100%**

E. Conclusion

Analysis of the loss in each layer provides motivation for future work and clear paths toward improving the performance of the LDs. The removal of one or more QWs from the 4 QW active region should have several benefits. The model shows modal loss in the QWs is high so fewer QWs will reduce the total loss in the structure. Additionally, fewer QWs will reduce the number of heterobarriers in the device, which should reduce the excess voltage and improve the uniformity of carrier injection into the active region.[37] Finally, the doping in *p*- and *n*-type layers could be further reduced to decrease the internal loss, provided that they do not have an impact on the electrical performance of the LDs.

In conclusion, CW blue semipolar $(20\bar{2}\bar{1})$ III-nitride lasers were fabricated using high quality facets produced by CAIBE etching. The internal loss and injection efficiency were measured to be 9 cm^{-1} and 73%, respectively, and the internal loss showed good agreement with simulated results of 9.5 cm^{-1}. The experimental results and the model provide details about the loss in the various epitaxial layers and can be used to guide future LD development.

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7. LD Results II: The Effect of Active Region Design on Gain and Carrier Injection and Transport

A. Introduction

Solid state lighting using laser diodes (LDs) is quickly gaining acceptance as a viable alternative to light emitting diode (LED) lighting.[1]–[4] LDs have much higher brightness than LEDs and can operate efficiently at much higher current densities. Additionally, the chip size of an LD can be much smaller than that of an LED, which combined with the high power of LDs can lead to dramatically reduced cost. However, as mentioned in proceeding chapters, InGaN LD wall-plug efficiency (WPE) remains lower than that of InGaN LEDs and that of other III-V LDs.[5]–[7] One way of improving the efficiency of InGaN LDs lies in the use of semipolar planes of GaN. These planes are predicted to have higher radiative efficiency and higher gain, arising from the higher wavefunction overlap (due to the reduction of polarization fields) and unbalanced biaxial stress leading to splitting of the top valence bands with an accompanying reduction in hole effective mass.[8]

B. Gain Curves

In particular, the semipolar $(20\bar{2}\bar{1})$ plane has lower polarization fields which also oppose the built in field of the p-n junction for InGaN devices emitting in the blue spectral range.[9] This

plane has been used to demonstrate high power LEDs and LDs.[10], [11] In the previous chapter, the measurement of internal loss in LDs grown on this plane using the cavity length dependent method was discussed.[12] Several routes to improving the LD performance were identified in that chapter, including reducing the number of quantum wells (QWs) in the active region. This was expected to reduce the internal loss of the LD because of the high modal loss from free carrier absorption in each QW, to reduce the operating voltage due to the removal of heterobarriers in the active region, and to reduce the threshold current by eliminating the transparency current for additional wells. By examining the gain curves for a series of LDs with differing numbers of QWs in the active region, this effect can be illustrated. A gain curve can be calculated from the loss and injection efficiency values obtained in the previous chapter.[12] The material gain, g_m, can be plotted versus injected current density (current density times injection efficiency), assuming uniform injection in the wells, for the 4 QW LD from Chapter 6 according to methods previously published.[13]–[15] Then with a simple two-parameter logarithmic fit to Eq. (7-1) using parameters from Chapter 6 of internal loss 9 cm^{-1} and injection efficiency 73 %, the transparency current density per well ($J_{tr,1}$ = 383 A/cm^2) and the gain parameter value, ($g_{0,1}$ = 6.36 cm^{-1}) can be extracted. The number of QWs, N_{QW}, was 4 and the confinement factor, Γ_{NQw}, was 3.2 % (0.8% per well) for the LD in Ref 12. Figure 7-1 shows this curve.

$$g_m = \frac{N_{QW}}{\Gamma_{N_{QW}}} g_{0,1} \ln[\frac{J}{N_{QW} * J_{tr,1}}] \qquad (7\text{-}1)$$

Then, according to Eq. (7-2), the modal gain curves (Γg) for samples with 4, 3, 2, and 1 QW(s) can be constructed by varying N_{QW} accordingly. These curves are seen in Figure 7-2.

$$\langle g_{N_{QW}} \rangle = \Gamma_{N_{QW}} g_m = N_{QW} g_{0,1} \ln[\frac{J}{N_{QW} * J_{tr,1}}] \qquad (7\text{-}2)$$

It is important to note that the assumptions implicit in this analysis are uniformly injected QWs and constant internal loss and injection efficiency with regards to cavity length across the LDs measured in our previous work. These may be poor assumptions, as will be discussed later in the chapter. This simple analysis predicts that active regions containing 2, 3, or 4 QWs should all perform similarly, and in light of the uncertainties and assumptions, the optimal well number is unclear. This motivated the present experimental study.

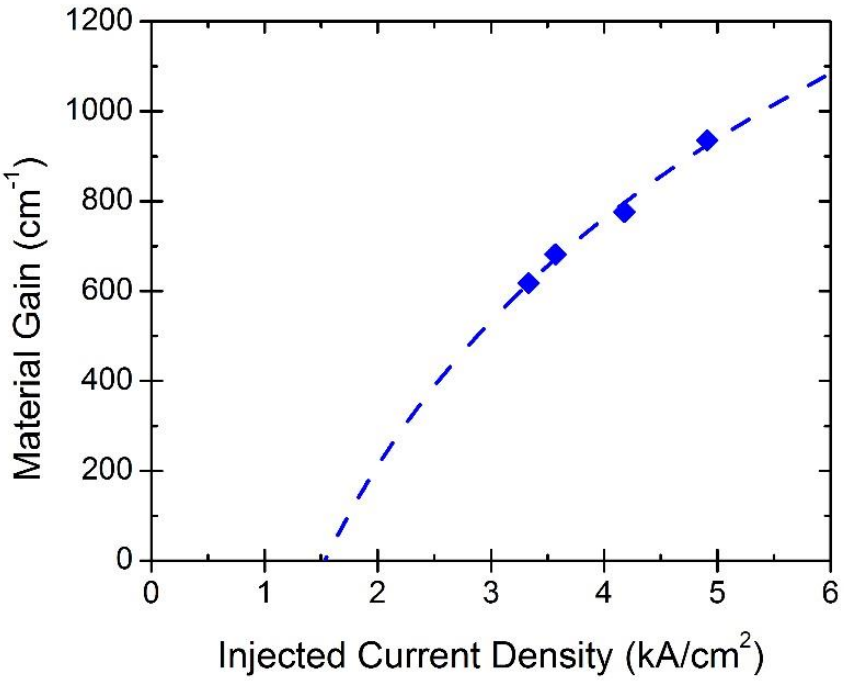

Figure 7-1: Material gain versus injected current density with a two parameter logarithmic fit calculated using Eq. (7-1) from data in Chapter 6. Copyright 2016 The Japan Society of Applied Physics[16]

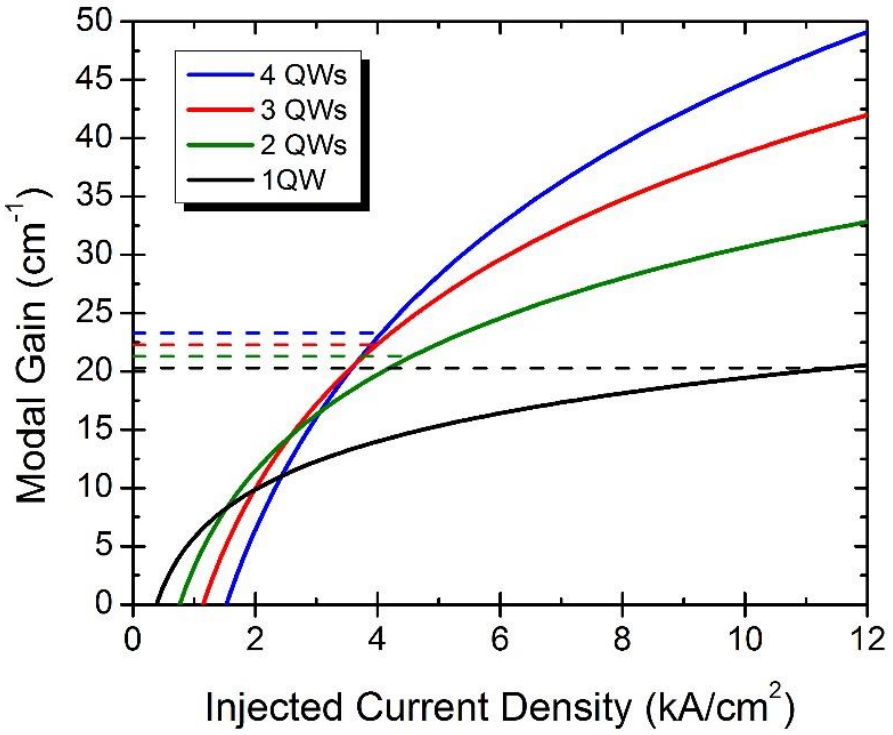

Figure 7-2: Gain curves for 1200 µm by 5 µm LDs with different active region designs calculated according to Eq. 7-2. The dashed lines are total loss of 1200 µm x 5 µm LD from Chapter 6 (assuming 1 cm-1 internal loss per well). Copyright 2016 The Japan Society of Applied Physics[16]

C. Experimental Procedure

LDs were grown using metal organic chemical vapor deposition (MOCVD) on free standing semipolar $(20\bar{2}\bar{1})$ bulk GaN substrates. Figure 7-3 shows the full epitaxial structure, similar to the one from Chapter 6 except for the number of QWs, which was varied from 1-4. Ridge waveguides were formed with reactive ion etching (RIE) etching, and SiO_2 was deposited as a field insulator using a self-aligned liftoff process. Pd/Au p-contacts and Ti/Au p-pads were deposited by electron beam evaporation. Facets were formed via Chemically Assisted Ion Beam Etching (CAIBE) according to an optimized procedure previously published.[17] A

blanket backside n-contact of Al/Ni/Au was deposited on the 330 μm thick substrate by electron beam evaporation. Then the samples were soldered with Pb/Sn/Ag solder onto a 1 cm^3 Cu block for continuous wave (CW) testing, which was then attached with a screw to a temperature-controlled stage. The LD lengths varied from 900 μm to 1800 μm and ridge widths were 5 μm.

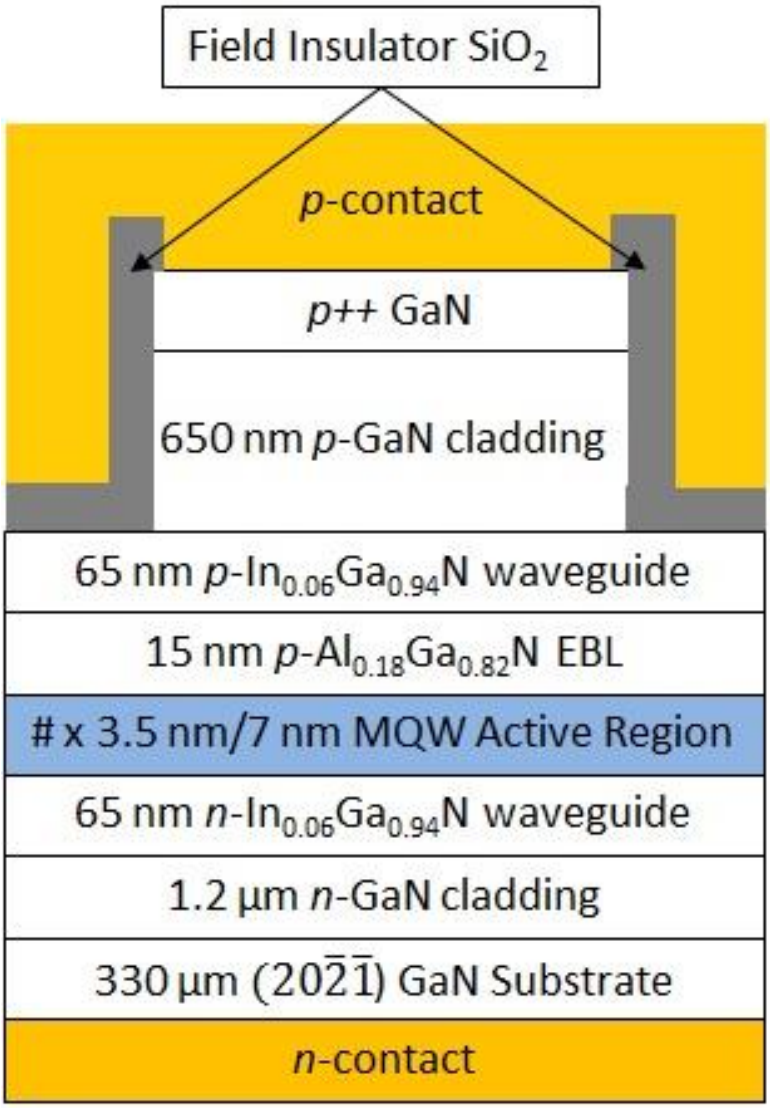

Figure 7-3: Epitaxial structure of the LDs. The # indicates the experimentally varied number of quantum wells from 1-4. Copyright 2016 The Japan Society of Applied Physics[16]

D. Results

A threshold current as low as 2.6 kA/cm^2 was obtained with an 1800 μm long LD containing 2 QWs. A light output power-current-voltage (L-I-V) curve for a 5 μm by 1200 μm LD lasing at 428 nm with a 2 QW active region is shown in Figure 7-4 for both pulsed (500 ns pulse width, 0.5% duty cycle) and CW testing conditions. The kink in the pulsed L-I curve is an observed lateral mode hop. Significant heating can be seen under CW operation. The measured voltage difference between CW and pulsed is due to heating, as well as the removal of probe resistance by using a 4 probe testing condition for the CW measurement. (Each probe adds approximately 1 ohm of series resistance in the 2 probe testing condition.) Peak power was 1366 mW (507 mW) under pulsed (CW) operation as measured from only one of the two uncoated facets. Assuming equal power from each facet, as was previously confirmed from uniform CAIBE facet etches[17], the two facet differential efficiency (η_d) was 54% (46%) under pulsed (CW) operation. The WPE was 11% at 1 A drive current under CW operation, a low value due to the rather high device voltage of 10 V at 1 A, to be discussed later. Thermal rollover is seen beyond this point on the CW L-I curve. Reduction of voltage and better thermal management should enable higher current and more efficient CW operation.

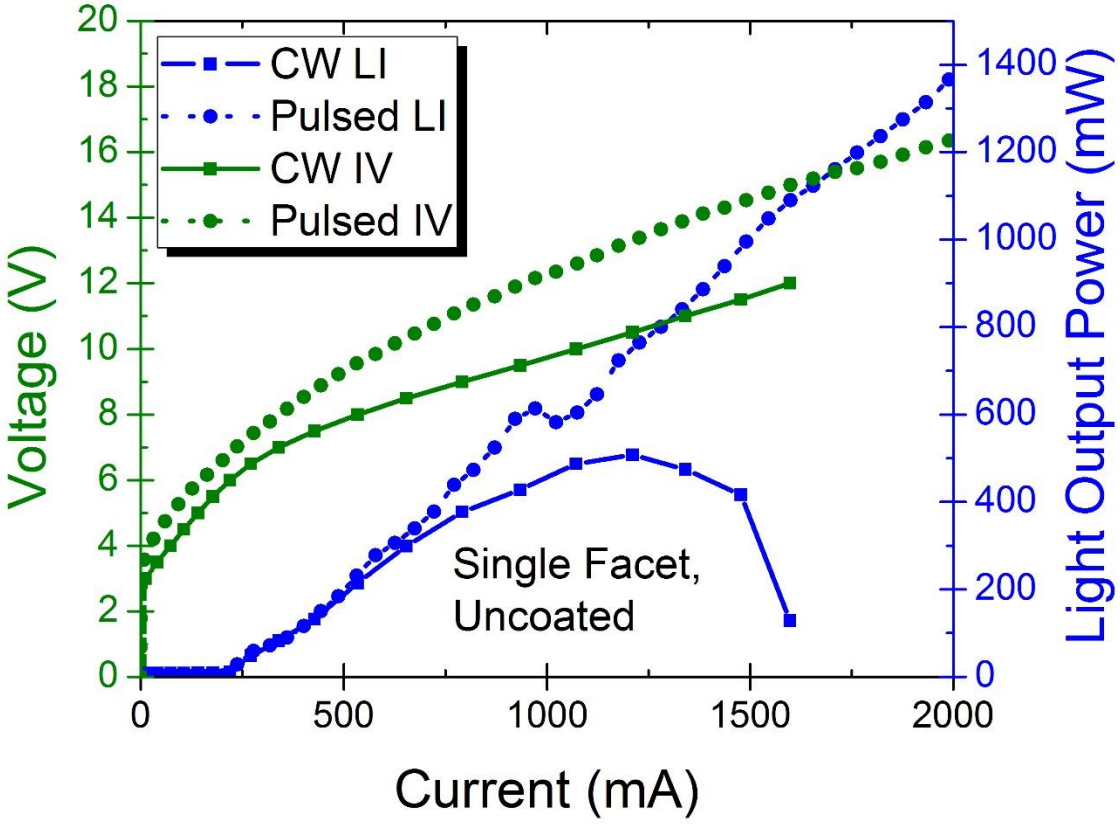

Figure 7-4: L-I-V curve for a high power 5 x 1200 µm 2 QW LD emitting at 428 nm under pulsed and CW testing, from only one uncoated facet. Copyright 2016 The Japan Society of Applied Physics[16]

The effect of varying the number of QWs on threshold current density (J_{th}) is shown in Figure 7-5. The multiple quantum well (MQW) samples showed a trend of decreasing J_{th} with decreasing number of QWs as expected from the lower transparency current. In contrast, the single quantum well (SQW) LDs showed the highest J_{th}. (The dashed lines are a simple exponential fit to guide the eye).

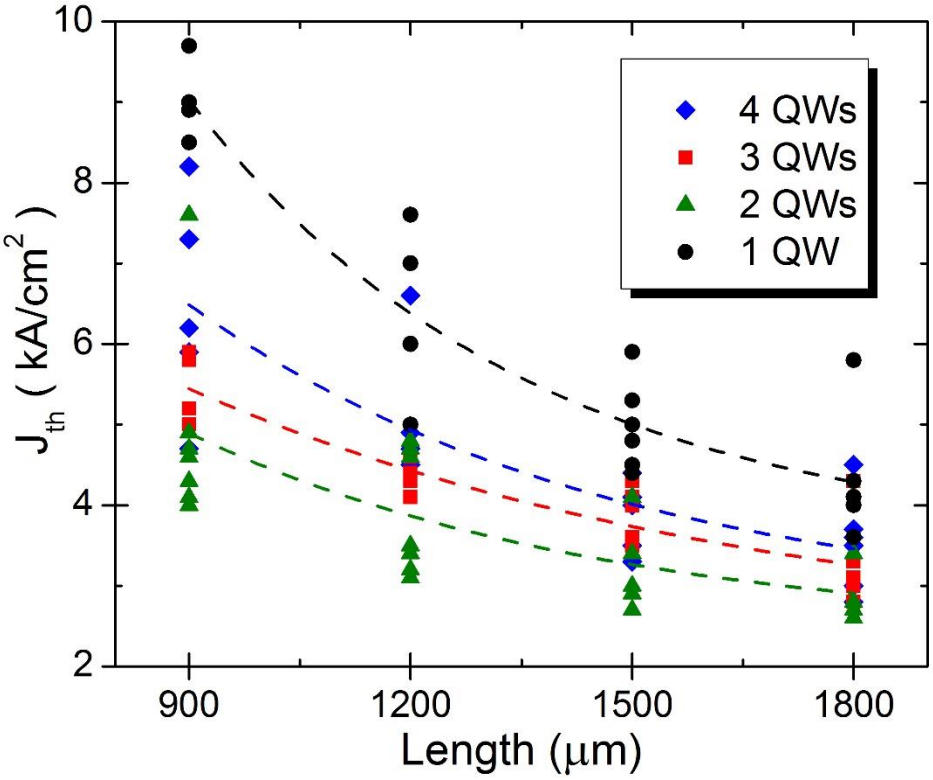

Figure 7-5: Threshold current density versus ridge length for 5 μm wide LDs with different active regions. Copyright 2016 The Japan Society of Applied Physics[16]

Temperature dependent measurements of the threshold current were done to investigate carrier transport in these active regions. Figure 7-6 shows the results of this measurement, and reported T_0 values, where T_0 is a characteristic temperature according to Eq. (7-3).

$$I_{th} = I_0 e^{T/T_0} \qquad (7\text{-}3)$$

T_0 increased monotonically with the number of wells, from a rather low value of 131K for the SQW laser, to 135K and 173K for the 2 and 3 QW samples. The 4 QW laser showed an unexpectedly high value of 555K over this temperature range.

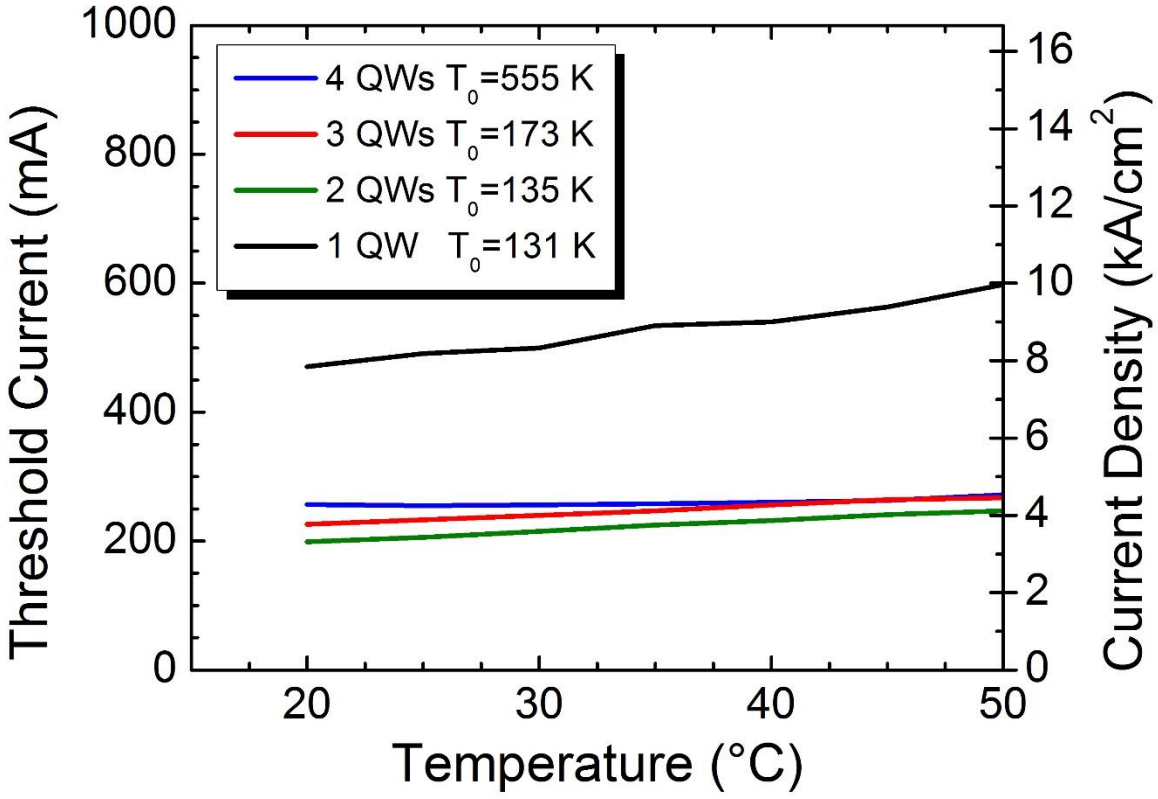

Figure 7-6: Threshold current versus temperature for the different LDs and T_0 values. Copyright 2016 The Japan Society of Applied Physics[16]

A high oxygen level in the p-AlGaN electron blocking layer (EBL) was found via secondary ion mass spectroscopy (SIMS). Figure 7-7 shows this measurement, with Mg, Si and O levels shown. The [O] level in the EBL was 4 x 10^{18} /cm^3, compared to the [Mg] level of 3 x 10^{19} /cm^3. This suggests the possibility of compensation of the magnesium acceptor by oxygen, which acts as a donor in GaN. Based on doping statistics, this could reduce hole concentration by an order of magnitude.[18] This could explain the leakage observed in these LDs. Previous studies of MOCVD growth on nonpolar and semipolar planes of GaN including $(10\bar{1}0)$, $(11\bar{2}2)$, $(10\bar{1}1)$, and $(10\bar{1}\bar{1})$ have shown an increased oxygen uptake compared to c-plane[19]

although oxygen incorporation in $(20\bar{2}\bar{1})$ AlGaN has not been studied. Possible avenues exist to reduce the oxygen level. This will be investigated further, and correcting this should reduce device voltage and improve injection efficiency.

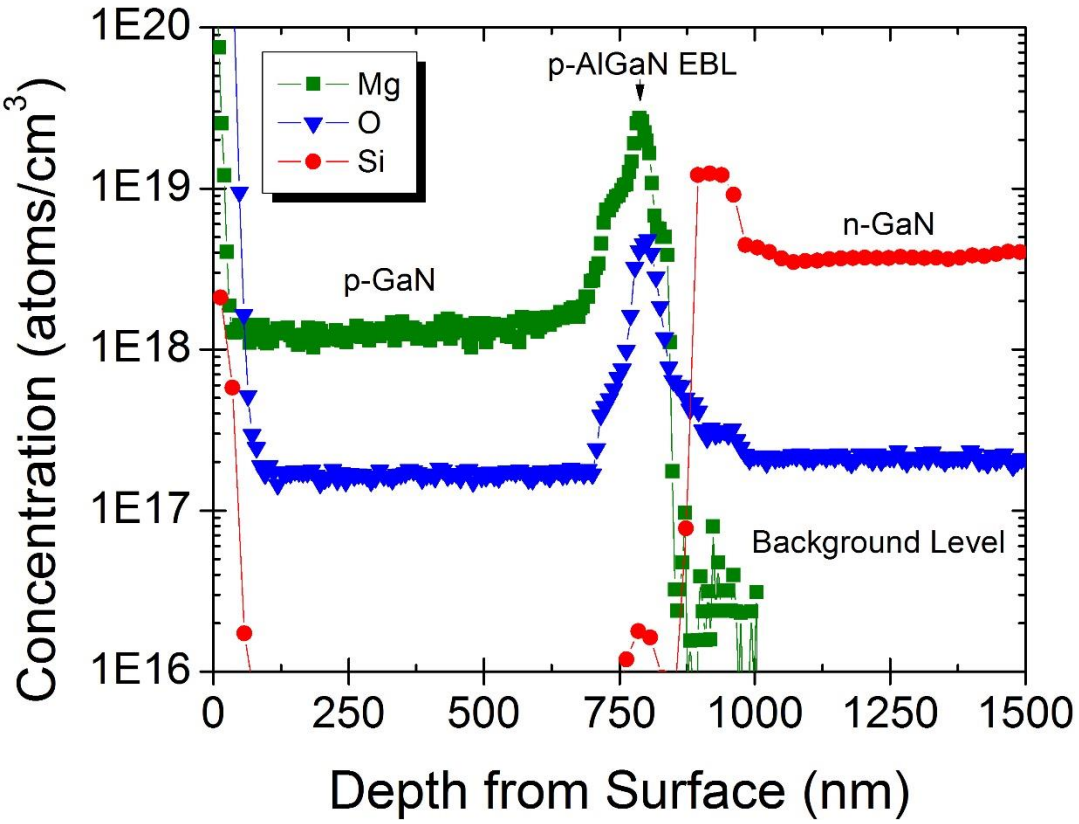

Figure 7-7: Secondary Ion Mass Spectroscopy (SIMS) measurement showing high oxygen level in p-AlGaN EBL. Copyright 2016 The Japan Society of Applied Physics[16]

E. Discussion

To understand these issues better, simulations of the band diagrams, carrier density in the QWs and gain per QW were done using SiLENSe LD version 5.10, a commercial drift-diffusion simulation tool from STR Group. All of the material parameters for each of the three binary III-N compositions used in the calculations are listed in tables in Appendix B. Their

values were selected after careful review of the literature and are available from the vendor's website, along with citations to the original experimental measurements.[20] Linear interpolation between the binary compositions was used for all parameters except band gap and electron affinity, for which published bowing parameters were used. The model included anisotropic effective masses and full calculation of the piezoelectric and spontaneous polarization fields for the $(20\bar{2}\bar{1})$ orientation. Default values from STR Group were used for all parameters except for spectral broadening, Auger recombination and hole mobility, as noted below. Gain calculations are always sensitive to the spectral broadening parameter and Auger recombination coefficient: spectral broadening of 40 meV was used because it reproduced the measured 20 nm electroluminescence spectral width at 1 kA/cm^2, and an Auger coefficient C=1.5 x 10^{-31} cm^6/s was used as a fitting parameter, but consistent with theoretical calculations by Kioupakis et al.[21] The results were also very sensitive to the electrical conductivity of the EBL. While accurate Mg and O concentrations from SIMS data were used, no accurate hole mobility data in the highly compensated AlGaN was available. Hole mobility in the EBL of 8 cm^2/V-s provided reasonable agreement with experimental threshold and differential efficiency results for the 4 QW laser at 20°C, and this same mobility value was used for all the simulations. The author thanks Dr. Daniel Cohen for conducting the simulations.

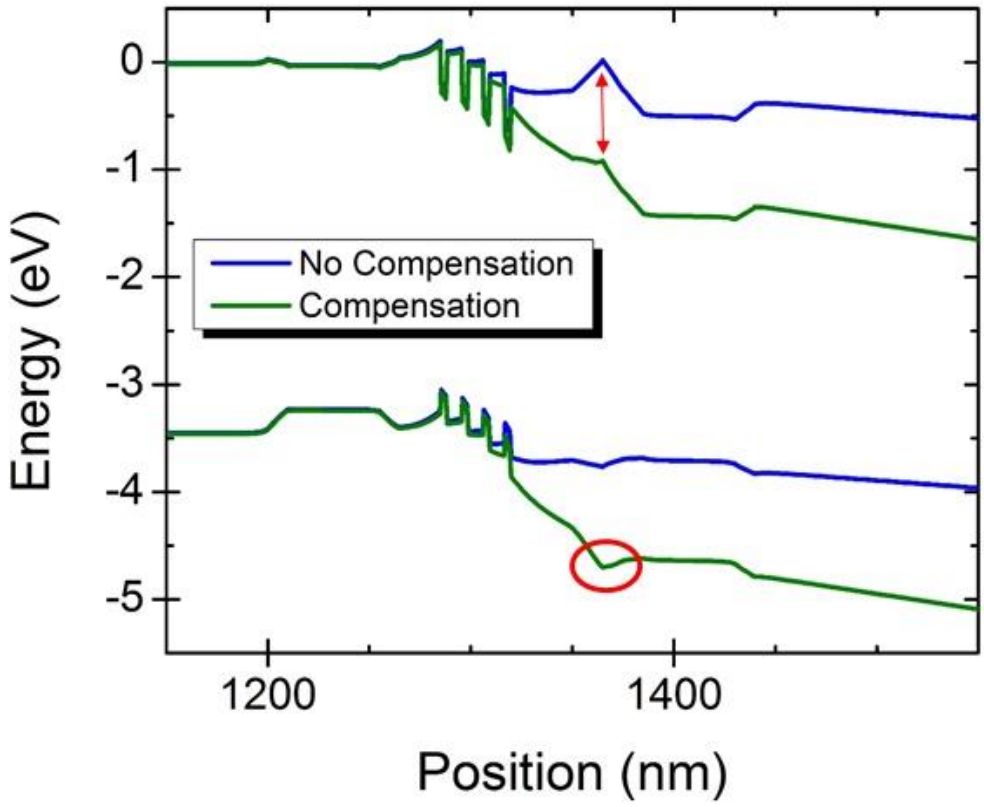

Figure 7-8: Band diagram for 4 QW showing the effects of the compensated EBL. A hole injection barrier and reduced electron leakage barrier are highlighted. Copyright 2016 The Japan Society of Applied Physics [16]

The results showed decreasing threshold current as the number of wells was reduced from four to two, but the results did not reproduce the dramatic increase in threshold for the single quantum well laser. Nor did the simulation replicate the relatively low T_0 values observed for the 1, 2, and 3 QW LDs. It was clear in the simulation that the voltage drop across the compensated EBL resulted in excessive carrier leakage out of the top well adjacent to the EBL and a barrier to hole injection, as seen in the biased band diagram of Figure 7-8. As the temperature was increased, the improved Mg activation raised the effective barrier height and

resulted in a very high or negative T_0. Such behavior has been reported before in InGaN lasers.[22]–[24]

More interesting is that the electron leakage from the topmost well of the 4 QW laser was so high that even at lasing threshold the well was far below population inversion, the excess loss nearly counteracting the gain available from the second and third wells. The top well of the 3 QW reached transparency, and both wells of the 2 QW provided significant gain. The leakage decreases as the number of QWs are reduced to 2, resulting in more equal carrier densities in the wells and more uniform gain. Figures 7-9, 7-10, and 7-11 show gain curves for each of these situations, 4, 3, 2 QWs respectively, with gain in each QW shown in green and total gain in blue. The magnitude of the voltage drop across the EBL depends on the total current, and a complicated relationship exists between transparency, Auger and leakage currents that might explain both the high T_0 of the 4 QW and the high J_{th} of the SQW lasers.

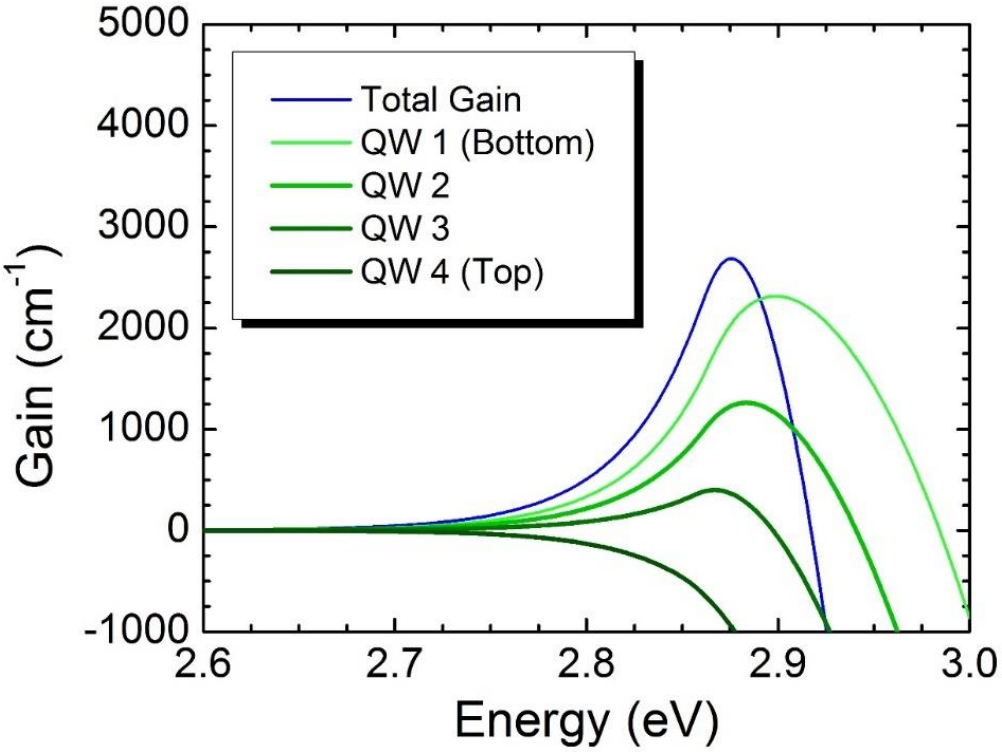

Figure 7-9: Simulation of gain curves for 4 QW LD Copyright 2016 The Japan Society of Applied Physics [16]

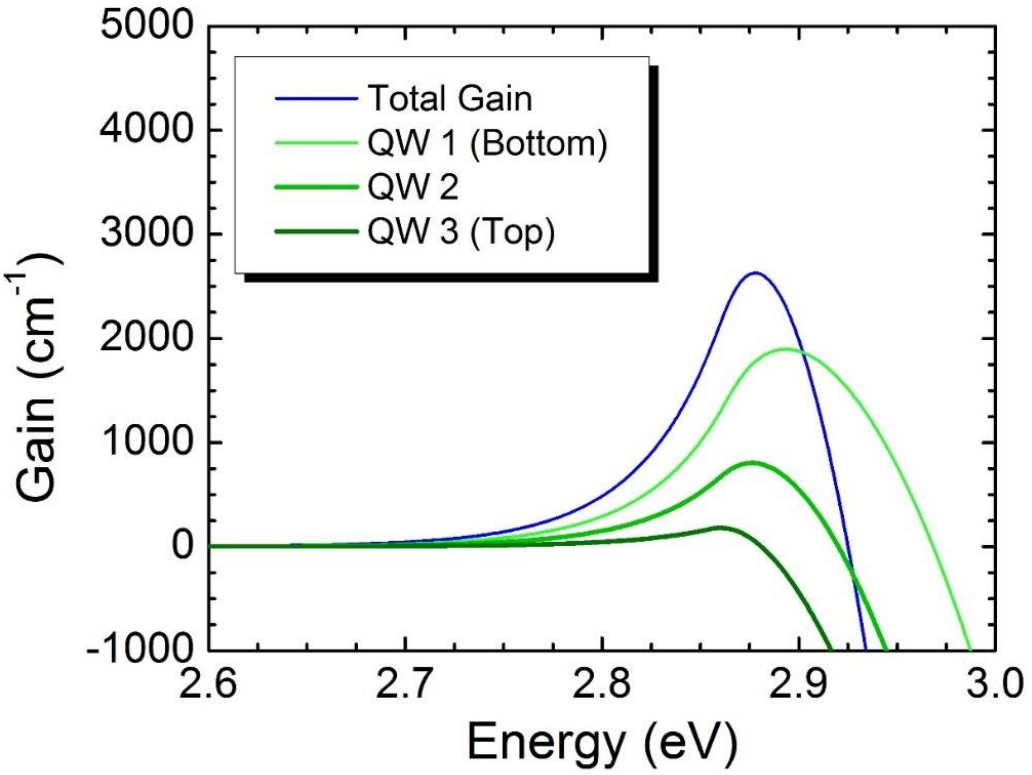

Figure 7-10: Simulation of gain curves for 3 QW LD Copyright 2016 The Japan Society of Applied Physics[16]

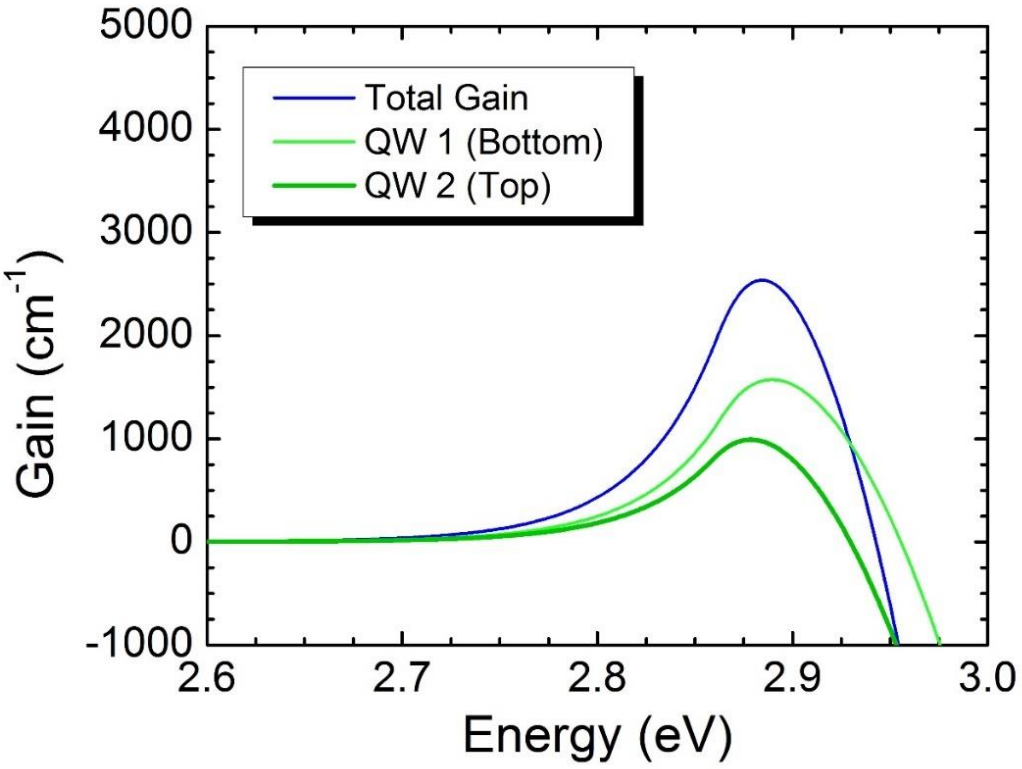

Figure 7-11: Simulation of gain curves for 2 QW LD Copyright 2016 The Japan Society of Applied Physics[16]

F. Conclusion

Semipolar laser diodes with improved performance were demonstrated using a 2 QW active region. Carrier leakage and carrier distribution nonuniformity are identified as possible causes of poor performance of the SQW and 3, 4 QW devices and the high device voltage across all LDs. An ineffective EBL compensated by oxygen could cause this leakage, which will be addressed in the next chapter.

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8. LD Results III: Characterization of Doping Compensation and Loss in $(20\bar{2}\bar{1})$ LDs

The previous chapter identified oxygen compensation as an issue in the EBL of the high power LD structure. This chapter will discuss by what mechanism the oxygen limits performance, how to reduce the oxygen level, and the improvements in device performance. More measurements of internal loss will also be discussed.

A. Oxygen Compensation Overview

The discussion in this section is based heavily on the dissertation of Peter Kozodoy from UCSB.[1] Mg forms a deep level in GaN, with acceptor binding energies on the order of 100-200 meV. In general, only about 1 % of Mg acceptors are ionized after activation in p-type GaN or AlGaN.[2] With the presence of a compensating donor, a certain number of acceptors must be ionized to cancel the charge of the compensating donors, this will pin the Fermi level at a particular energy. Since $p << N_D < N_A$, the number of ionized acceptors equals the number of ionized donors, which is constant, and this will fix the Fermi level and the

number of holes available as well. Figure 8-1 illustrates this effect for various compensation ratios (N_D/N_A).

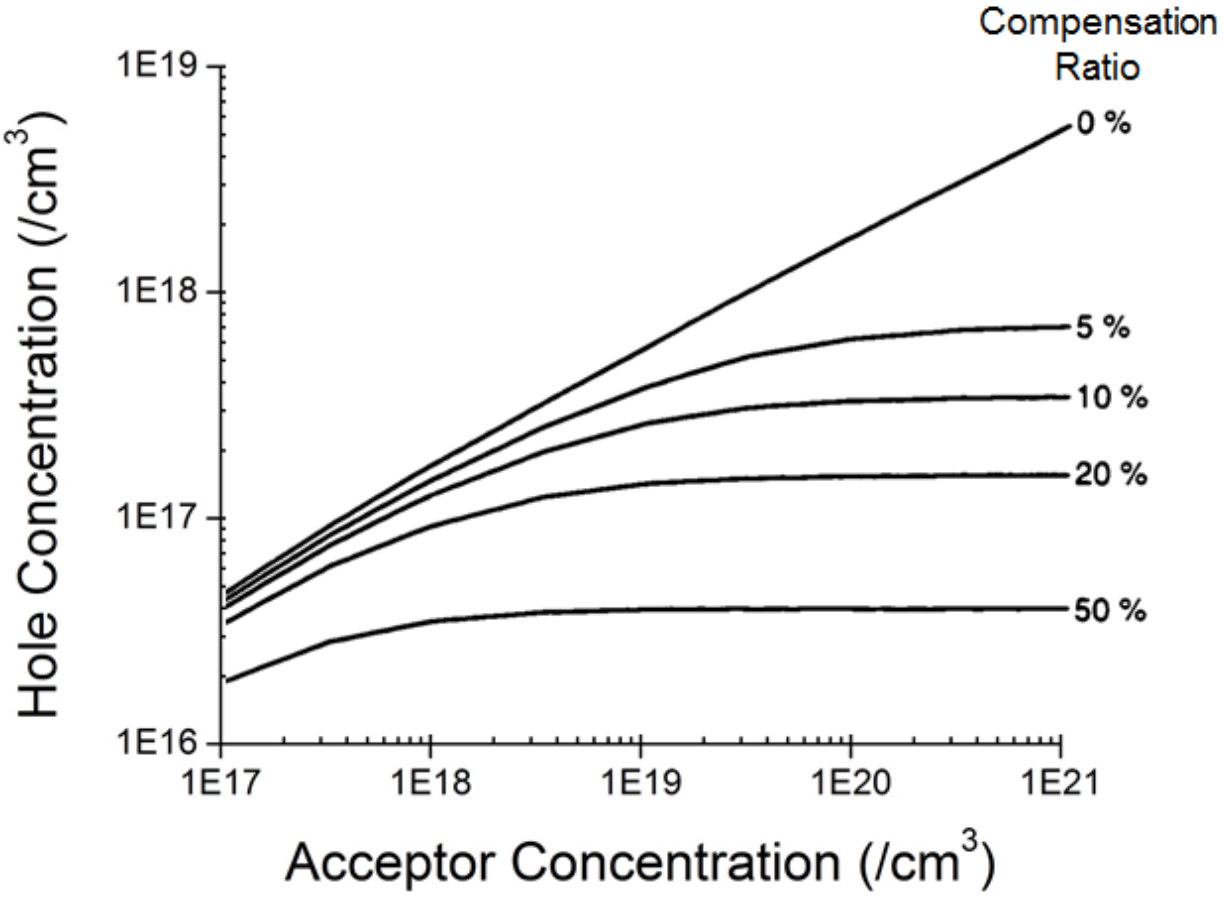


Figure 8-1: Compensation Effect on Hole Concentration (adapted from P. Kozodoy Dissertation 1999)[1]

Oxygen was identified as a compensating donor in the AlGaN electron blocking layer in the LDs presented in the previous chapter. At high doping levels employed in the devices mentioned in the previous chapter, the presence of a compensating donor will reduce the hole concentration from 2 x 10^{18} /cm^3 to 2 x 10^{17} /cm^3. SiLENSe simulations confirm that the oxygen present in the EBL will cause a high amount of electron leakage and a hole injection barrier. A simulated I-V curve is shown in Figure 8-2. It shows the effect of compensation on

the I-V turn on and series resistance. An experimental curve is overlaid (the dotted line) showing much better agreement with the compensated case than the uncompensated case.

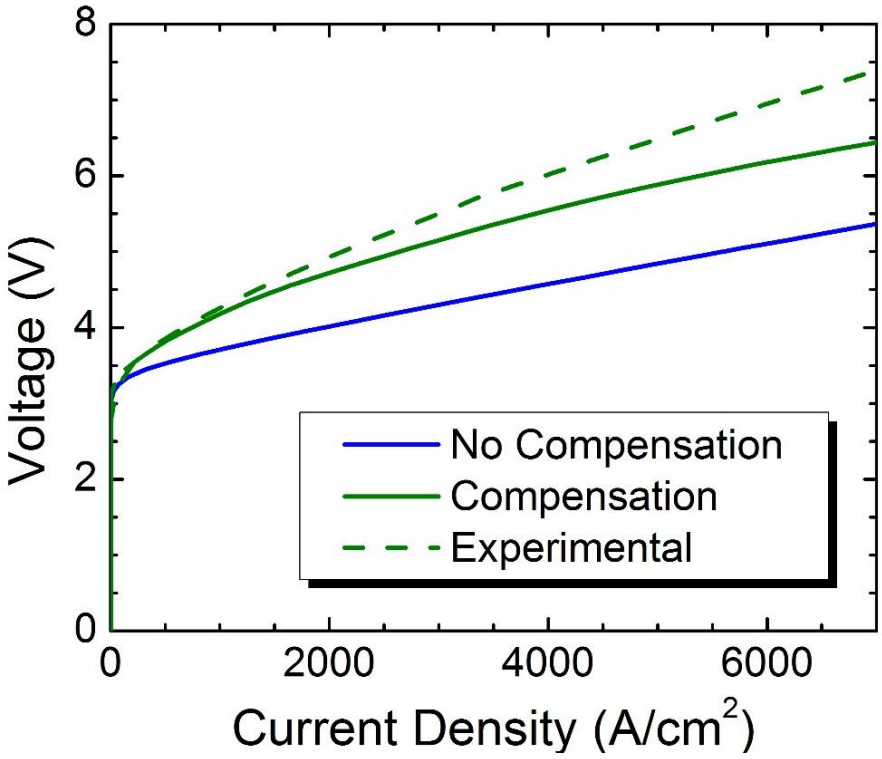


Figure 8-2: Simulated I-V Curve showing Compensation Effect

B. Experimental Results in Reducing Oxygen

Several groups have reported increased impurity incorporation for samples grown on semipolar planes of GaN versus that on c-plane.[3]–[5] This is suggested to occur due to the nanofaceted step-flow growth scheme observed for semipolar planes.[6] These groups have also discussed ways of reducing oxygen. Several of these ideas will be presented in this section, and then their effect on oxygen levels in semipolar AlGaN will be presented.

Cruz et al. identify an increase in V/III ratio as reducing oxygen impurities since oxygen incorporates on nitrogen lattice sites. They also discussed increasing the growth

temperature since the Ga-O bond is less favorable at high temperatures. A third method possible is reducing any sources of residual oxygen present in the reactor. The use of a sapphire wafer as a corral for growth on semipolar planes could contribute oxygen as the sapphire is heated in the presence of NH_3. These three methods are investigated in this section.

The effect of increasing temperature is shown in Figure 8-3.

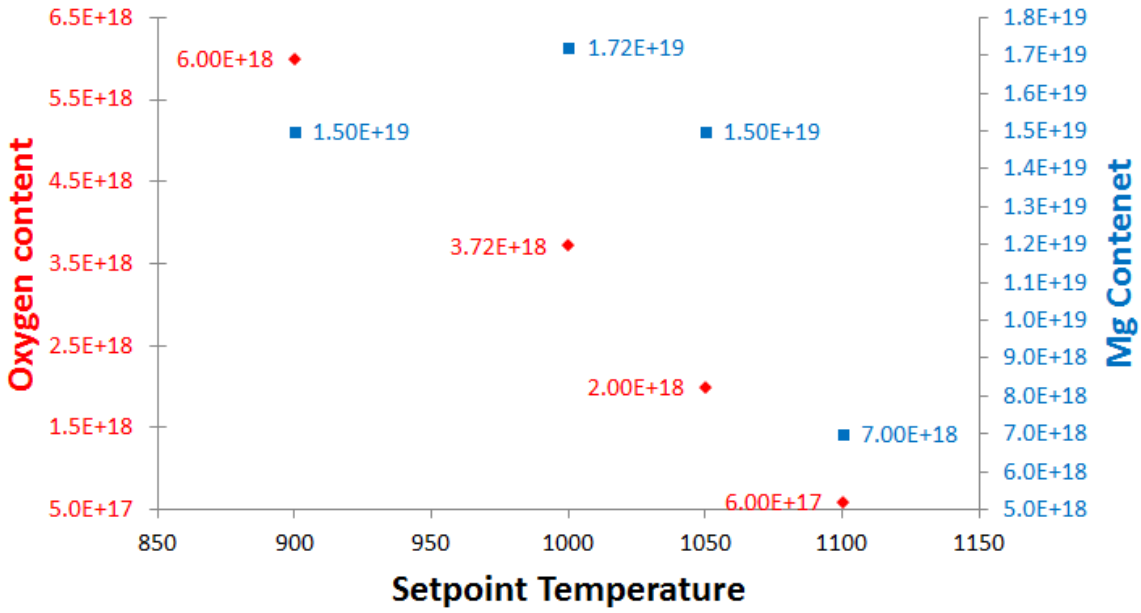


Figure 8-3: Temperature Effect on [Mg] and [O]

The oxygen content did indeed decrease with increasing temperature, however the Mg incorporation also decreased. This kept the overall compensation level approximately the same. Thus this route was not effective. The V/III ratio increase likewise did not impact the compensation ratio. However, the removal of the sapphire corral had a large impact, as can be seen in Figure 8-4, a plot of the compensation ratio at various growth conditions both with and without sapphire present.

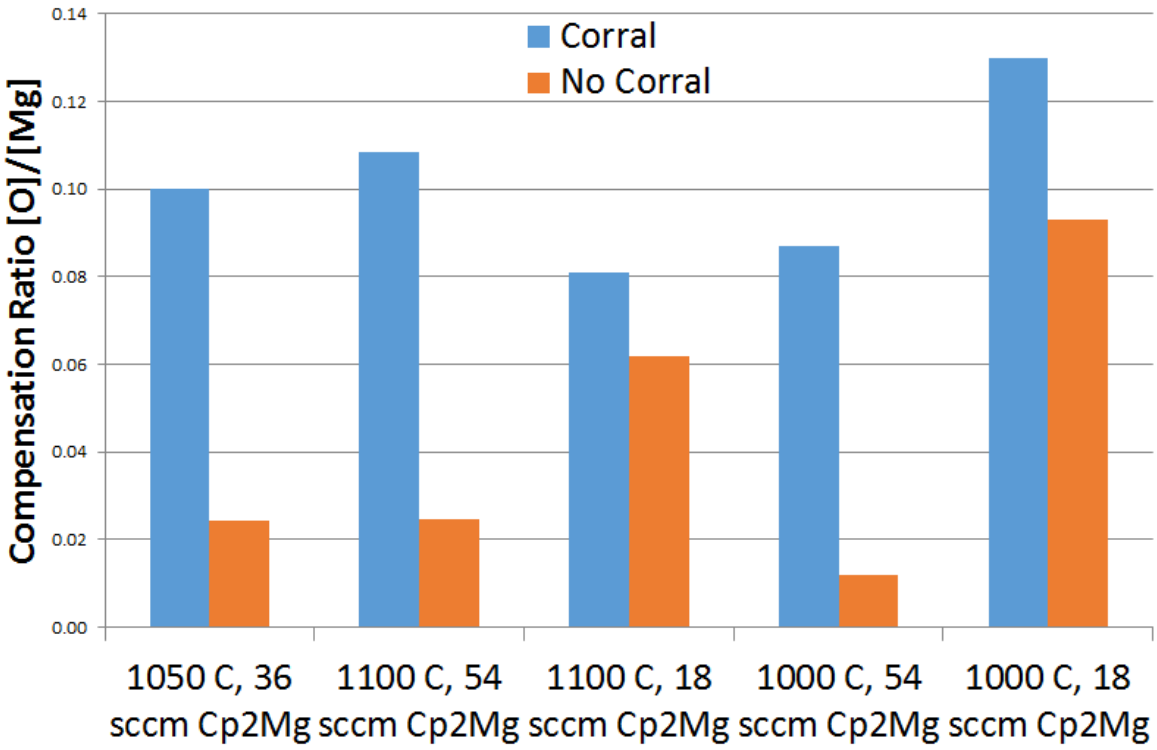


Figure 8-4: Compensation Ratio Reduction by Removal of Corral

Then the final oxygen level at a Mg concentration of 3 x 10^{19} /cm^3 is reduced from 4 x 10^{18} /cm^3 to 5 x 10^{17} /cm^3. This reduces the compensation ratio to 2%, sufficient for LD use.

C. Laser Results for Improved p-contact and Reduced Oxygen Conditions

LDs were fabricated with similar structures to the 2 QW device presented in Chapter 7. The difference was in the targeted wavelength of 410 nm for the LD, so the QW compositions was shifted to about 12% In, and the waveguiding layer compositions were shifted to about 4 % In. The wavelength adjustment was selected with applications in mind and will be discussed in Chapter 9. Figure 8-5 shows the epitaxial structure. Identical LDs were grown, one with the sapphire corral and one without. Figure 8-6 shows the I-V characteristic for these lasers.

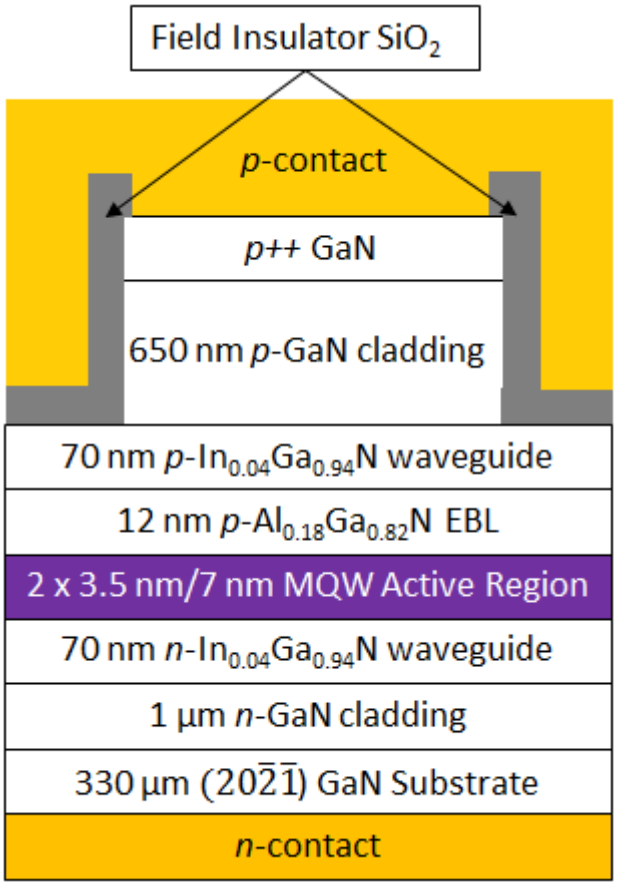


Figure 8-5: Laser Structure

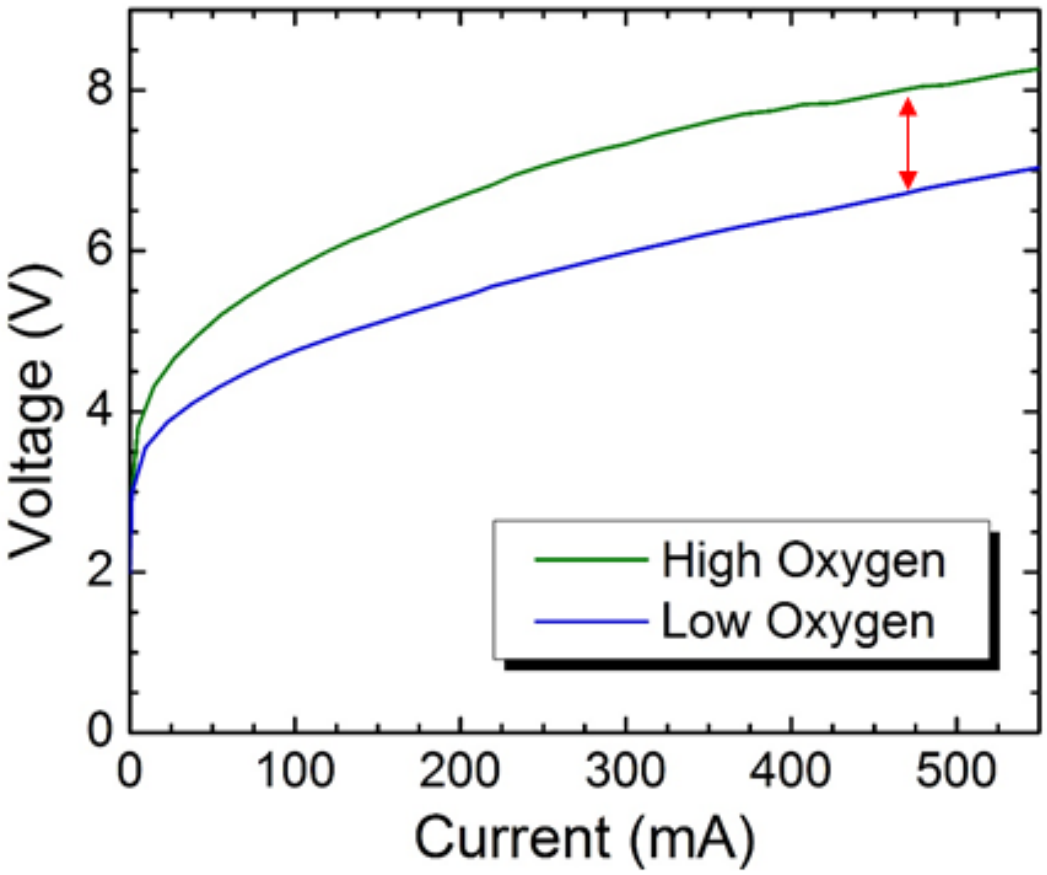


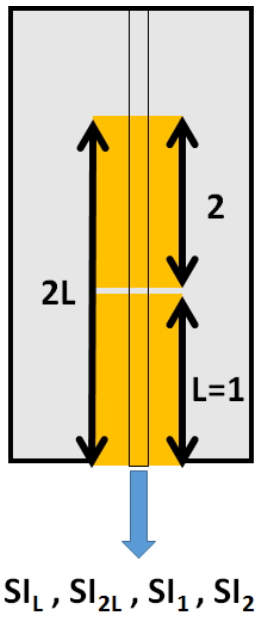
Figure 8-6: I-V showing voltage reduction with oxygen reduction

The voltage is substantially reduced. However, lasing behavior was observed at very high current densities of tens of kA/cm^2, so more work is needed to verify the improvement.

D. Further Internal Loss Measurements: Segmented Contact

This section will briefly discuss an additional measurement of internal loss, the segmented contact method, which was performed on the lasers with the structure presented above. The segmented contact measurement allows a measurement of internal loss from one laser structure, so it can overcome some of the limitations of the cavity length dependent method, namely the typically flawed assumption that loss and injection do not vary across several devices.[7] The segmented contact method uses a single laser waveguide, with two identical

metal contacts separated with a few microns. In this measurement, the contacts were 300 μm long, with a 3 μm gap in between them. The ridge continues far past the second contact, so as to be considered absorbing. The facet at the other edge, in front of the first contact, is etched at a slight angle to ensure no feedback is provided. Then from the facet one can measure amplified spontaneous emission. By taking measurements of the spectral intensity with segment 1, 2, or both biased, one can measure gain and loss spectra according to Figure 8-7.



$$(\Gamma g - \alpha_i) = \frac{1}{L} * \ln[\frac{SI_{2L}}{SI_L} - 1]$$

$$(\Gamma \alpha - \alpha_i) = \frac{1}{L} * \ln[\frac{SI_1}{SI_2}]$$

Spectral Intensity 1L gain = $SI_L = SI_1$
Spectrum with only the first segment biased

Spectral Intensity 2L gain = SI_{2L}
Spectrum with both segments biased

Spectral Intensity 1L absorption = SI_2
Spectrum with only second segment biased (first segment absorbing)

Figure 8-7: Segmented Contact Measurement Details

Figure 8-8 shows the results of this measurement for the structure shown in Figure 8-5. The lasing wavelength was 405 nm. The internal loss was estimated to be 12 – 14 cm^{-1} from where the loss and gain curves converge at low photon energies (longer wavelength).[7] The thick lines with circles are the Modal Gain- Modal Loss, and the thin solid lines are Modal Absorption- Loss.

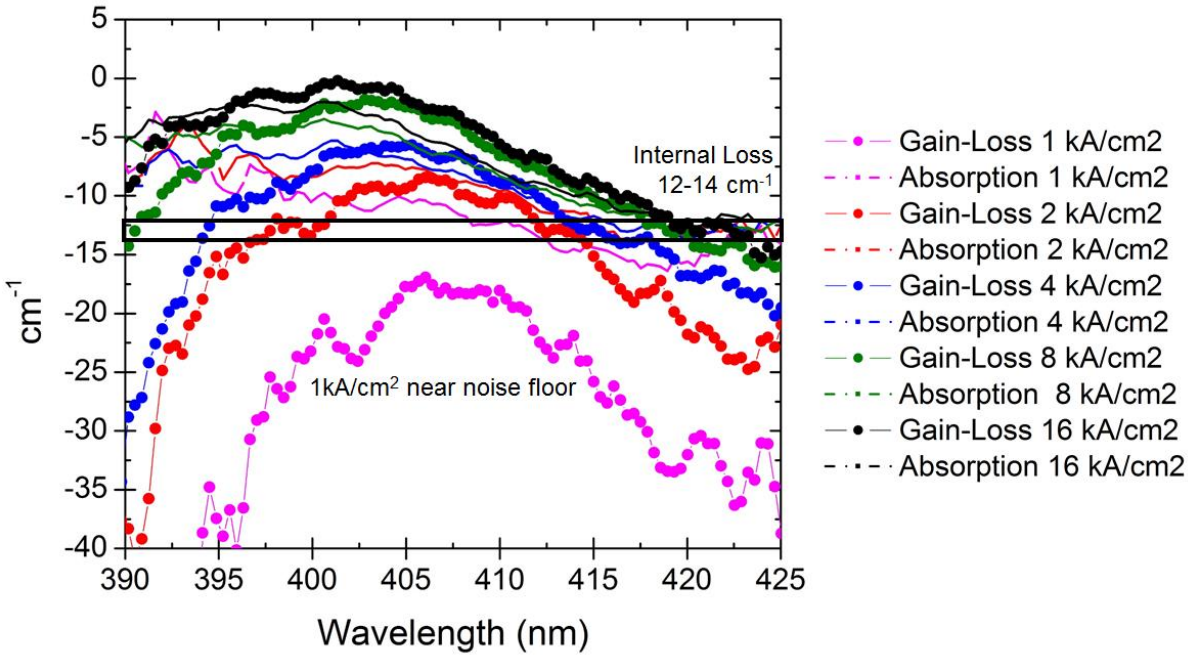


Figure 8-8: Modal Gain - Loss and Modal Absorption from Segmented Contact Measurement

The measurement of internal loss shows a good agreement with the predicted internal loss of about 10 cm^{-1}. Note that the 1 kA/cm^2 (and to lesser extent 2 kA/cm^2) curve does not converge at longer wavelengths as expected from theory. This is suggested to be because of the high noise floor from the experimental setup used (ocean optics spectrometer, some ambient light). Further optimizations of the experimental setup should address this issue.

E. Conclusion

The mechanism of oxygen compensation was reviewed in this chapter, and a low oxygen growth scheme was presented. Devices were fabricated using this scheme, and lower voltage was seen. The changes to the laser structure meant that the laser performance could have

been affected, so more research must be done. An internal loss measurement was also presented.

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9. Summary and Future Work

There are several routes to higher WPE semipolar LDs. Several possibilities will be discussed in this chapter, before the dissertation is summarized.

A. Best 2 QW LD Revisited

The simulation of internal loss for the 2 QW device from Chapter 7 is shown in Figure 9-1.

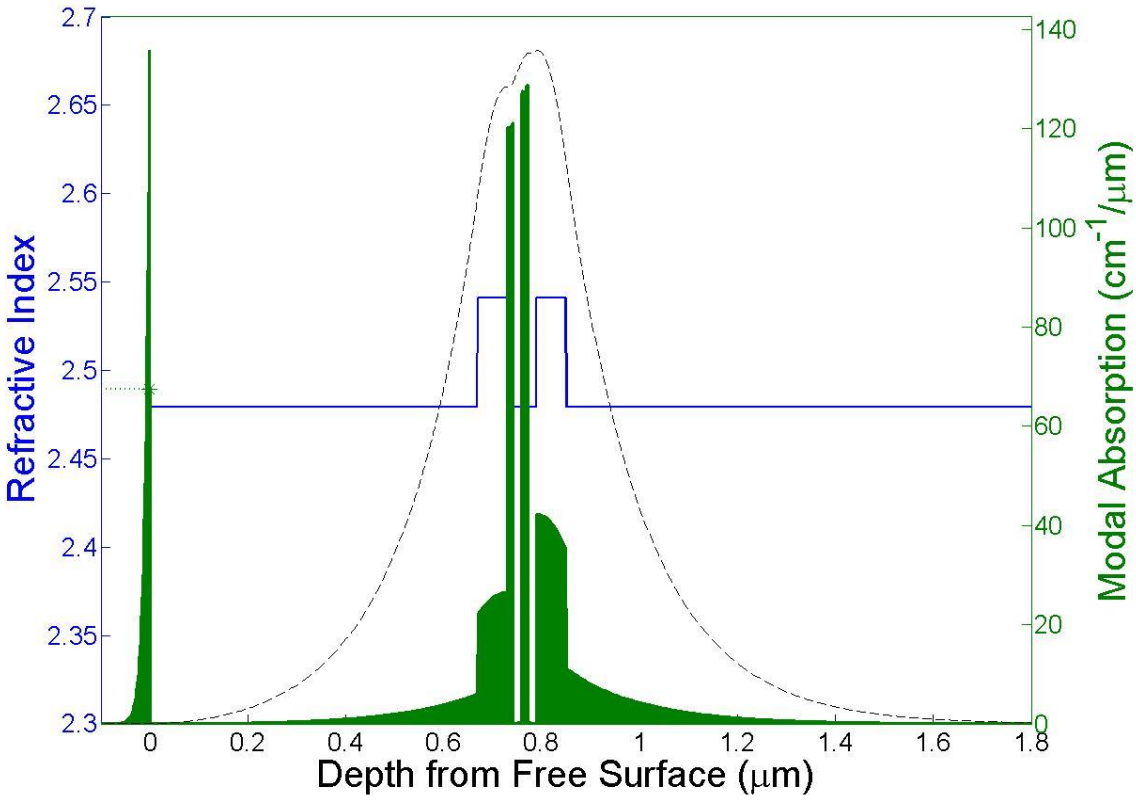

Figure 9-1: Simulation of 2 QW LD at 440 nm

The confinement factor was 3.9 %. The wavelength was 440 nm. The green shaded areas are the areas of loss. Total loss was calculated to be 10 cm^{-1}, based on most current measurements of thickness and doping. Refractive indices from STR were used, see Appendix B for more information. The breakdown of loss in each layer can be seen in Table 9-1. Significant free-carrier/dopant absorption loss can be seen in the InGaN waveguiding layers, as well as the n-cladding layer. These should be simple to reduce by reducing the doping concentration. The dopant concentration in these three layers is quite high, so reducing it should not have a significant impact on voltage. The next section will present a simple route to reducing internal loss to 4 cm^{-1}.

Table 9-1: Loss for 2 QW LD

Layer	Composition	With latest data Thickness	3.9 % CF Doping	440 nm Loss in Each Layer
Pd	Pd	180	--	1.30
p++ GaN	GaN	10	1.00E+20	0.00
p+ GaN	GaN	10	1.00E+19	0.00
p- GaN cladding	GaN	650	1.70E+18	0.88
p-InGaN waveguide	$In_{0.04}Ga_{0.93}N$	60	5.00E+18	1.50
p- AlGaN EBL	$Al_{0.18}Ga_{0.82}N$	12	3.00E+19	1.45
GaN Barrier	GaN	10	1.00E+17	0.00
GaN Barrier	GaN	7	1.00E+17	0.00
InGaN QW-2	$In_{0.11}Ga_{0.82}N$	3	p=n=1e19	0.38
GaN Barrier	GaN	7	1.00E+17	0.00
InGaN QW-1	$In_{0.11}Ga_{0.82}N$	3	p=n=1e19	0.39
GaN Barrier	GaN	7	1.00E+17	0.00
GaN Barrier	GaN	10	1.00E+17	0.00
n-InGaN waveguide	$In_{0.04}Ga_{0.93}N$	60	1.00E+19	2.40
n-GaN cladding	GaN	1200	4.00E+18	1.76
GaN substrate	GaN	300	1.00E+17	0.00
			Total	10.07

Figure 9-2 shows the WPE breakdown of this laser. It is clear that both differential efficiency and voltage efficiency must be improved. The next section describes how internal loss can be reduced to improve the differential efficiency.

$$\text{WPE} = 11\%,$$
$$P_{max} = 1.1\text{W} @ 1\text{A} @ 10\text{ V}$$
$$\text{slope effic. } 1.34\text{ W/A}$$
$$\eta_{th} = 82\%$$
$$\eta_{d} = 46\%$$
$$\eta_{V} = 28\%$$

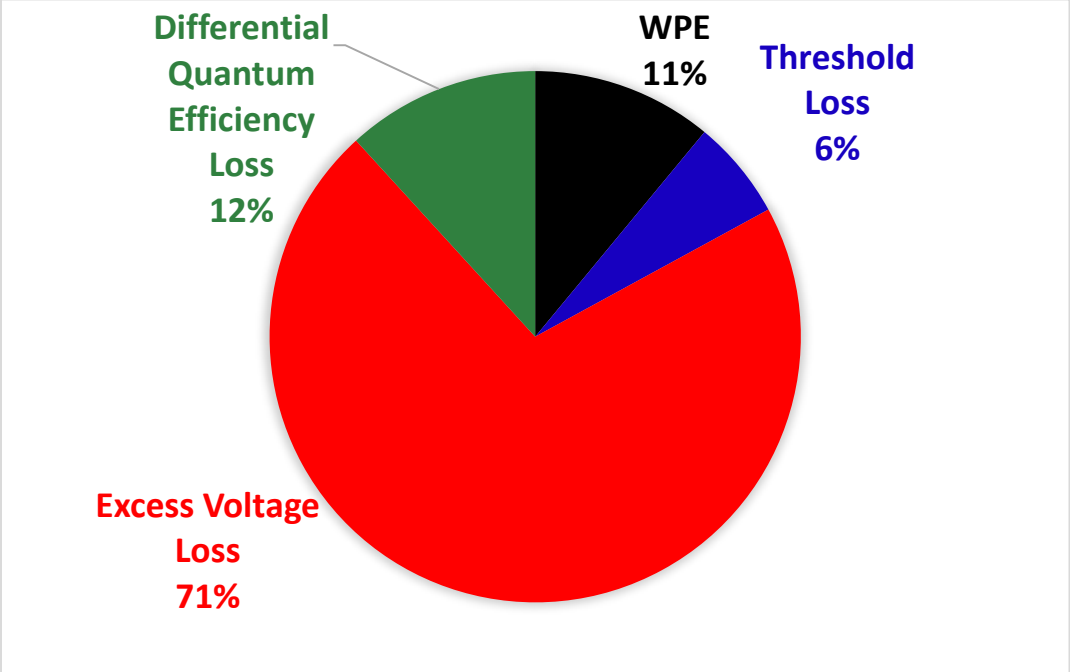

Figure 9-2: WPE Breakdown of Best 2 QW LD

The voltage loss dominates in this LD. We can further estimate the contribution to excess voltage (~ 7 V total at 1 A) from various sources as follows: 4 V of Schottky barrier like ~3 V from the p-contact and ~1 V from heterobarriers in the epitaxial structure, and 3 V of ohmic loss, with ~1.5 V from the substrate, ~1 V from the p-contact, and ~0.5 V from the p-GaN cladding. Later sections will discuss how these voltages could be reduced.

B. Reducing Internal Loss

This section will present the route to 4 cm^{-1} internal loss. By reducing the doping levels in the cladding and waveguiding layers, it can be achieved. A recent paper from Panasonic suggests this will have a negligible effect on electrical performance.[1]

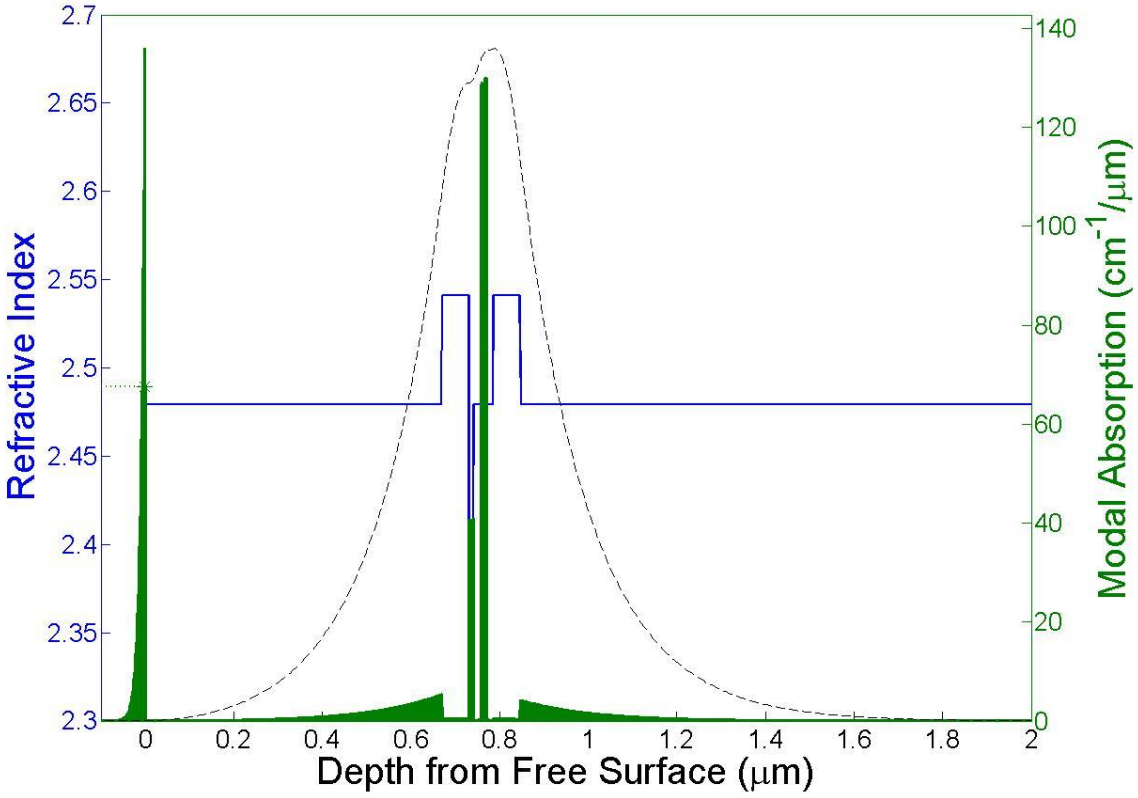

Figure 9-3: Mode Profile for 440 nm LD with low loss

Figure 9-3 shows the new mode profile, and Table 9-2 shows the values used and loss in each layer. The reduced values are bolded.

Table 9-2: Loss in Each Layer for Updated LD Structure

Layer	Composition	Thickness	Doping	440 nm Loss in Each Layer
Pd	Pd	180	--	1.30
p++ GaN	GaN	10	1.00E+20	0.00
p+ GaN	GaN	10	1.00E+19	0.00
p- GaN cladding	GaN	650	**1.50E+18**	0.78
p-InGaN waveguide	$In_{0.04}Ga_{0.93}N$	60	**1.00E+17**	0.03
p- AlGaN EBL	$Al_{0.18}Ga_{0.82}N$	12	**1.00E+19**	0.49
GaN Barrier	GaN	10	1.00E+17	0.00
GaN Barrier	GaN	7	1.00E+17	0.00
InGaN QW-2	$In_{0.11}Ga_{0.82}N$	3	p=n=1e19	0.39
GaN Barrier	GaN	7	1.00E+17	0.00
InGaN QW-1	$In_{0.11}Ga_{0.82}N$	3	p=n=1e19	0.39
GaN Barrier	GaN	7	1.00E+17	0.00
GaN Barrier	GaN	10	1.00E+17	0.00
n-InGaN waveguide	$In_{0.04}Ga_{0.93}N$	60	**1.00E+17**	0.02
n-GaN cladding	GaN	1200	**1.50E+18**	0.66
GaN substrate	GaN	300	1.00E+17	0.00
			Total	4.08

The sources of loss now are the penetration of the mode into the metal contact, the EBL, the cladding layers, and the QWs. In the next section, addressing the loss in the metal and the QWs will be addressed. It is harder to address loss in the EBL since electron leakage has been shown to be a problem, but it will also be discussed in the following section.

C. Improving Waveguiding and Confinement

As mentioned in the introduction, the goal of the project was to improve wall-plug efficiency. Reducing the internal loss would improve the differential efficiency and lower the threshold current density. Internal loss could be reduced further by introducing a TCO such as ITO to improve confinement.[2] Eliminating one of the two QWs could reduce loss further. Figure 9-4 shows the impact of these two changes, and Table 9-3 shows the loss in each layer, with total loss 2.6 cm^{-1}.

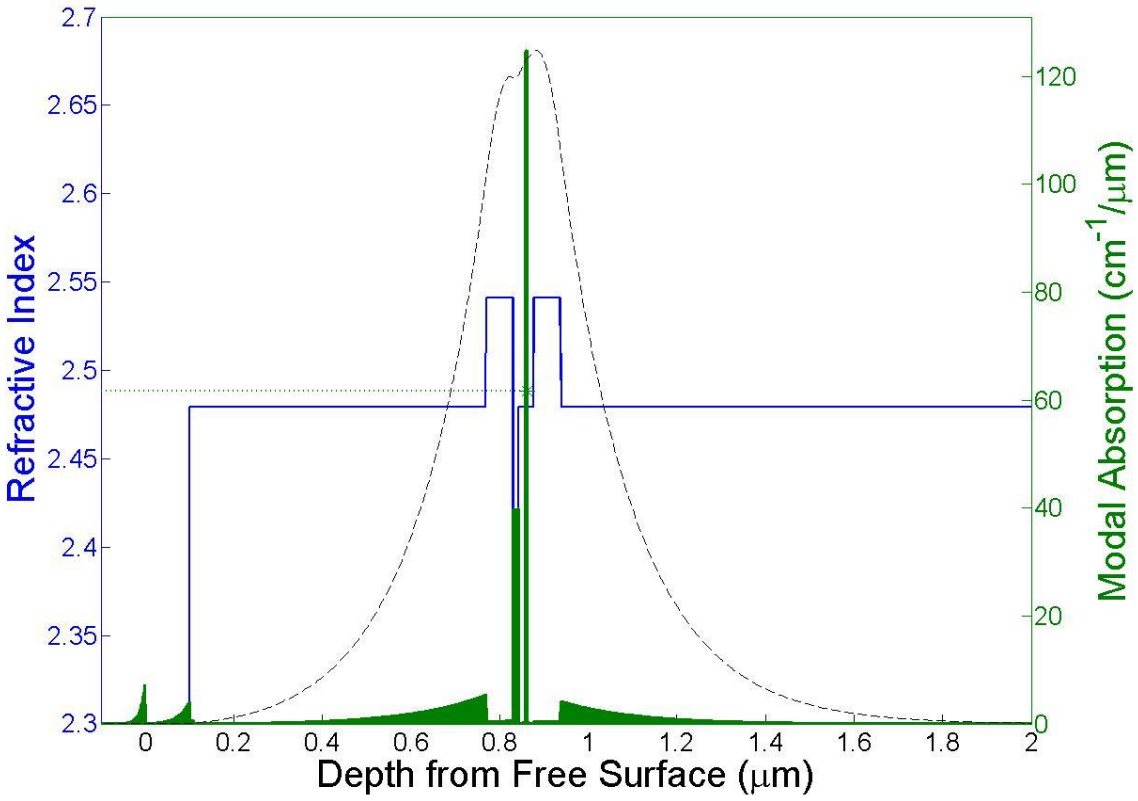

Figure 9-4: Mode Profile for SQW ITO LD

Table 9-3: Loss in Each Layer for SQW ITO LD

Layer	Composition	Thickness	Doping	440 nm Loss in Each Layer
Pd	Pd	180	--	0.09
ITO	ITO	100	2000cm^{-1}, index 2.09	0.10
p++ GaN	GaN	10	1.00E+20	0.01
p+ GaN	GaN	10	1.00E+19	0.00
p- GaN cladding	GaN	650	1.50E+18	0.83
p-InGaN waveguide	$In_{0.04}Ga_{0.93}N$	60	1.00E+17	0.03
p- AlGaN EBL	$Al_{0.18}Ga_{0.82}N$	12	1.00E+19	0.48
GaN Barrier	GaN	10	1.00E+17	0.00
GaN Barrier	GaN	7	1.00E+17	0.00
InGaN QW-1	$In_{0.11}Ga_{0.82}N$	3	p=n=1e19	0.37
GaN Barrier	GaN	7	1.00E+17	0.00
GaN Barrier	GaN	10	1.00E+17	0.00
n-InGaN waveguide	$In_{0.04}Ga_{0.93}N$	60	1.00E+17	0.02
n-GaN cladding	GaN	1200	1.50E+18	0.69
GaN substrate	GaN	300	1.00E+17	0.00
			Total	2.62

ITO may also have superior current spreading or resistance by reducing the thickness of p-GaN cladding, this must be confirmed with experiment. ZnO could also be used.[3] P- contacts could be further improved by annealing or alternate metallization; this must be investigated further.[4], [5]

D. Reducing Voltage and Thermal Impedance

The voltage penalties identified in section 9-A can be addressed systematically. The biggest loss is in the p-GaN contact. Current p-GaN contacts to semipolar $(20\bar{2}\bar{1})$ have specific contact resistivities on the order of 10^{-4} Ω-cm^2. [6] This should be reduced to the 10^{-6} Ω-cm^2 for a negligible voltage penalty at high current operation. This has been shown before in the

literature for c-plane GaN.[4], [7] The removal of QWs, waveguiding layers and/or the EBL, as well as grading the composition or doping at layer transitions, will lower these barriers, but they cannot be totally eliminated. Ohmic losses from finite bulk resistances in the p-GaN cladding and substrate can be limited by thinning these layers out. Using ITO or ZnO (previous section) or a tunnel junction (next section) could allow the p-GaN cladding to be thinned. The largest ohmic loss in the present structure is the 330 μm thick substrate. By thinning the substrate or using a topside n-contact, this loss could be reduced.

Additionally, the thermal impedance of the GaN substrate contributes to the heating under CW operation. From the temperature dependent measurement of the threshold current and comparison of pulsed and CW operation presented in Chapter 7, a thermal impedance of 13 °C/W was extracted. This agreed well with the calculated thermal impedance of the GaN substrate of 11 °C/W according to the model in Chapter 2 of Coldren et. al.[8] By thinning the substrate to 70 μm before metallization and soldering to a heatsink, the thermal impedance could be reduced nearly in half. This will allow for high current CW operation with accompanying increase in power out.

E. Advanced Designs for High Power, High Efficiency

There are a number of advanced designs to push efficiency higher. UCSB recently demonstrated LDs with a tunnel junction contact with hybrid MBE/MOCVD growth method.[9], [10] With the use of optimized n-contacts, the p-GaN contact, which is a major limiting factor to voltage performance, could be eliminated and a low contact resistance n-contact could be used on both the n and p side. The incorporation of any tunnel junction into a laser must be done carefully, since the highly doped layers of the tunnel junction could

contribute high absorption loss. This could be managed if the tunnel junction is far away or if it is fully depleted.

Additionally, the EBL could be moved further from the active region, as in a recent paper from Panasonic[1], or even removed. Further advanced waveguide designs could be used, such as those used in high power GaAs lasers, where the mode is shifted into the n-type layers since the p and QW layers contribute loss. These extreme double asymmetric (EDAS) designs are used in the highest performance lasers.[11], [12] In order to realize this design, a high index contrast top cladding is required. ITO could be used, but it contributes significant loss, and the refractive index difference may not be high enough. Recent developments in so-called porous GaN could provide a solution by offering GaN with a much lower refractive index.[13], [14]

F. Wavelength Selection for Solid State Lighting

The pump wavelength of traditional solid state lighting is around 450 nm. Recently issues have been identified relating to "blue light hazard," which refers to retinal damage from long exposure to high intensity blue light (peaking at 430 nm), and the melatonin suppression of LED light (where the response peaks at 490 nm). Much research is inconclusive or contradictory, so careful attention must be paid to sources. The Department of Energy at present does not believe there to be sufficient scientific evidence to warrant LED redesigns, reminding that the CCT and spectral power density can be tuned for various applications.

G. Conclusion

Many methods of improving the WPE of semipolar GaN LDs have been presented in this chapter. Reducing internal loss is the first step, and voltage inefficiencies must be addressed at

the contacts and substrate especially. Good thermal management should improve threshold efficiency. All of the steps outline show a path to world record InGaN WPE.

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Appendix A: Processing Manuals

Laser processing manuals are included here. Included are: Original Process, Topside n-contact ITO, and CAIBE Etched facet processes.

Etched Facet Ridge Process V4 - Standard Process
Last revised: 12/09/2010
R. M. Farrell, D. A. Haeger, P. S. Hsu

Project Step	Equipment	ID #	Process Step
Activation	AET RTA	1	700C, N2/O2, 15min
Ridges Litho	Solvent bench	2	1min Ace, 1min Iso, 1min DI, N2 dry
	PR Bench	3	Dehydration bake on hotplate at 110C for 2min, let cool 1min
		4	Spin LOL 2000, 2krpm/s, 10krpm/s^2, 30s (~350 nm thick)
		5	Clean backside of sample with EBR 100
		6	Bake on hotplate at 210C for 5min, let cool for 2min
		7	Spin 955CM-1.8, 3krpm, 10krpm/s, 30s (~1.8um thick)
		8	Clean backside of sample with EBR 100
		9	Soft bake on hotplate 95C for 90s
	GCA AutoStep 200	10	Load mask #1A/B/C/D/E - Ridges
		11	Load sample onto 2" 500um chuck with 200um shim with C+ pointing up
		12	Run "EXEC RIDGESV4A" (multiple plate) or "EXEC RIDGESV4B" (single plate)
		13	Pass: 1A/B/C/D/E (RIDGESV4A) or RIDGES (RIDGESV4B)
		14	No pass shift
		15	Expose 0.4s, focus=+2
	PR Bench	16	Post-exposure bake on hotplate at 110C for 90s
	Develop Bench	17	Develop in 726MIF for 75s (~15nm/s undercut after reaching 45s)

	Microscope	18	Inspect (verify ~0.3-0.5um undercut on LOL 2000), develop more if necessary
	UV Ozone	19	20min (~6A/min)
	Dektak	20	Dektak RIDGES pad
Ridges Etch	RIE #5	21	Load bare carrier wafer
		22	O2: 50sccm, 50mT, 300W, 10min (optional: He cooling: 5 sccm)
		23	BCL3/Cl2: 20/5sccm, 10mT, 15W, 3min (optional: He cooling: 5 sccm)
		24	Cl2: 10sccm, 5mT, 200W, 2min (optional: He cooling: 5 sccm)
		25	Unload carrier wafer
		26	Optional: Mount sample on carrier wafer with Santovac oil and reload carrier wafer
		27	BCL3: 10sccm, 10mT, 100W, 2min (optional: He cooling: 5 sccm)
		28	Cl2: 10sccm, 5mT, 200W, ~5-8min (~100-150nm/min) (optional: He cooling: 5 sccm)
		29	Carefully remove oil on backside of sample with Ace (if necessary)
		30	Soak sample in DI water for 2min, N2 dry
	Microscope	31	Inspect
	Dektak	32	Dektak RIDGES pad
SiO2 Dep & Liftoff	Veeco IBD	33	Co-load sample with Si monitor
		34	12_RMF_TF_SiO2_15deg, 15deg tilt, rot ON, ~2105s, ~200nm (~0.95 A/s)
	Ellipsometer	35	Measure Si Monitor #1 thickness
	Microscope	36	Inspect
	Solvent bench	37	Soak sample in 1165 heated to 80C for 10 min, agitate with pipette
		38	Sonicate in bath at frequency: 8, intensity: 8, power: low, time~20-30sec
		39	Soak sample in 1165 heated to 80C for 5 min, agitate with pipette
		40	2min Iso, 30s x 3 rinse & dump DI, N2 dry
	Microscope	41	Inspect, repeat steps 44-46 if necessary
	Dektak	42	Dektak RIDGES pad
Contact Pads Litho	Solvent bench	43	1min Ace, 1min Iso, 1min DI, N2 dry
	PR Bench	44	Dehydration bake on hotplate 110C 2min, let cool 1min

		45	Spin HMDS, 3krpm, 10krpm/s, 30s (let HMDS sit for 20s before spinning)
		46	Spin OCG825, 3krpm, 10krpm/s, 30s (~1.5um thick)
		47	Clean backside of sample with EBR 100
		48	Bake on hotplate at 95C for 2min
	MJB-3 (left aligner only)	49	Load sample onto one of the black chucks
		50	Flood expose 1s
	PR Bench	51	Let sample outgas for 5min (VERY IMPORTANT)
		52	Bake on hotplate at 95C for 2min, let cool 1min
		53	Spin 955CM-1.8, 3krpm, 10krpm/s, 30s (~1.8um thick)
		54	Clean backside of sample with EBR 100
		55	Softbake on hotplate at 95C for 90s
	GCA AutoStep 200	56	Load mask #2 - P-contacts
		57	Load sample onto 2" 500um chuck with 200um shim with C+ pointing up
		58	Run "EXEC RIDGESV4B"
		59	Pass: PCONTS
		60	No pass shift
		61	Expose 0.4s, focus=+2
	Develop bench	62	Develop in 726MIF for 60s (~2um undercut on OCG825)
		63	30s x 3 rinse & dump DI, N2 dry
	Microscope	64	Inspect, develop more if necessary
	UV Ozone	65	20min (~6A/min)
	Dektak	66	Dektak CONTACTS pad
Contact Pads Dep	Acid Bench	67	Mix 1:1 HCl:DI
		68	Etch sample in 1:1 HCl:DI for 30s
		69	30s x 3 rinse & dump DI, N2 dry
	E-beam #3	70	Deposit 300/10000A Pd/Au
	Solvent bench	71	Liftoff in 1165 heated to 80C for 10+ min, agitate with pipette
		72	Move sample to fresh beaker of 1165
		73	Soak sample in 1165 heated to 80C for 2min, agitate with pipette
		74	2min Iso, 2min DI, N2 dry
	Microscope	75	Inspect, repeat 1165 if necessary
	Dektak	76	Dektak CONTACTS pad
Facets Litho	Solvent bench	77	2min Ace, 2min Iso, 2min DI, N2 dry

	PR Bench	78	Dehydration bake on hotplate at 110C for 2min, let cool 1min
		79	Spin LOL 2000, 3krpm, 10krpm/s, 30s (~200nm thick)
		80	Clean backside of sample with EBR 100
		81	Bake on hotplate at 190C for 5min, let cool for 2min
		82	Spin SPR220-3.0, 2.5krpm, 10krpm/s, 30s (~2.7um thick)
		83	Clean backside of sample with EBR 100
		84	Bake on hotplate at 115C for 90s
	GCA AutoStep 200	85	Load mask #3 - Etched Facets
		86	Load sample onto 2" 500um chuck with 200um shim with C+ pointing up
		87	Run "EXEC RIDGESV4B"
		88	Pass: FACETS
		89	Expose 0.65s, focus=0
	PR Bench	90	Bake on hotplate at 115C for 90s
	Develop bench	91	Develop in 726MIF for 75s
	Microscope	92	Inspect (verify ~0.5-0.7um undercut on LOL 2000), develop more if necessary
	UV Ozone	93	20min (~6A/min)
	Dektak	94	Dektak FACETS pad
Facets Etch	Acid Bench	95	Mix 1:1 BHF:DI
		96	Etch piece of Si Monitor #1 in 1:1 BHF:DI (~300nm/min)
		97	Inspect monitor for hydrophobicity every 10-15s, record total etch time
		98	Etch sample in 1:1 BHF:DI for double the monitor etch time
		99	1 min DI, N2 dry
	RIE #5	100	Load bare carrier wafer
		101	O2: 50sccm, 50mT, 300W, 10min (optional: He cooling: 5 sccm)
		102	BCL3/Cl2: 20/5sccm, 10mT, 15W, 3min (optional: He cooling: 5 sccm)
		103	Cl2: 10sccm, 5mT, 200W, 2min (optional: He cooling: 5 sccm)
		104	Optional: Mount sample on carrier wafer with Santovac oil and reload carrier wafer

		105	BCL3: 10sccm, 10mT, 100W, 2min (optional: He cooling: 5 sccm)
		106	Cl2: 10sccm, 5mT, 200W, ~15min (~100-150nm/min) (optional: He cooling: 5 sccm)
		107	Soak sample in DI for 2min, N2 dry
	Solvent bench	109	Strip mask in PRX heated to 80C for 10+ min, agitate with pipette
		110	Move sample to fresh beaker of PRX
		111	Soak sample in PRX heated to 80C for 2min, agitate with pipette
		112	2min Iso, 2min DI, N2 dry
	Microscope	113	Inspect, repeat PRX if necessary
	Dektak	114	Dektak FACETS pad
N-contact Dep & Liftoff	PR Bench	115	Mount sample upside down on Si wafer with a drop of AZ 4110
		116	Bake on hotplate at 100C for 5min
	E-beam #3	117	Deposit 500/3000A Al/Au
	Solvent bench	118	Soak sample in 1165 heated to 80C until sample detaches from Si wafer
		119	2min Iso, 2min DI, N2 dry
	Microscope	120	Inspect, repeat 1165 if necessary

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Project Step	**Equipment**	**#**	**Process Step**
Remove Indium	Acid Bench	1	Mix 1:3 HNO_3:HCL (aqua regia) heated to 80 °C, repeat 2×[a]
		2	Etch sample in aqua regia for 5 min or more
(Optional) Reactivate	MOCVD lab furnace	3	Reactivate in 15 min at 600 °C (or use RTA N2/O2 for 15 min at 600 °C)
Ridges Litho	Solvent bench	4	3 min Ace, 2 min Iso, 1 min DI, N2 dry (sonicate on high)
	PR Bench	5	Dehydration bake on hotplate at ≥110 °C for ≥2 min, let cool 1 min
		6	Spin LOL 2000, 2 krpm, 10 krpm/s, 30s (~250 nm thick)
		7	Clean backside of sample with EBR 100
		8	Bake on hotplate at 210 °C for 5 min, let cool for 2 min
		9	Spin 955CM-1.8, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)
		10	Clean backside of sample with EBR 100
		11	Soft bake on hotplate 95C for 90s
	GCA Stepper[b]	12	Load mask Ridges
		13	Load sample onto 2" 500 µm chuck with 180 µm shim, *c*+ pointing up
		14	Double check the program die size, run "EX RIDGESTOPN"
		15	Pass: RIDGES
		16	Verify Pass shift (verify key offset to comp)
		17	Stepper 2:Expose 0.75s, focus=+2 Stepper 1: Expose 2.15 s, focus=0

	PR Bench	18	Post-exposure bake on hotplate at 110 °C for 90 s
	Develop Bench	19	Develop in 726MIF for 65 s
	Microscope	20	Inspect (verify ~0.3-0.5 µm undercut on LOL 2000), develop more if necessary
	UV Ozone	21	20 min (~6 Å/min)
	Dektak	22	Dektak RIDGES pad
Ridges Etch	RIE #5	23	Load bare carrier wafer
		24	O2: 50 sccm, 50 mT, 300 W, 10 min, no He cooling
		25	BCL3/Cl2: 20/5 sccm, 10 mT, 15 W, 3min, no He cooling
		26	Cl2: 10 sccm, 5 mT, 200 W, 2 min, no He cooling
		27	Load sample(s) on carrier wafer (no mounting oil)
		28	BCL3: 10 sccm, 10 mT, 100 W, 2 min, no He cooling
		29	Cl2: 10 sccm, 5 mT, 200 W, ~1-5min (~120 ± 10 nm/min, target 100 nm above QWs/90% of p-GaN cladding), no He cooling
		30	Soak sample in DI water for 2 min, N2 dry
	Microscope	31	Inspect
	Dektak	32	Dektak RIDGES pad
SiO2 Dep & Liftoff	Sputter #3	33	Co-load sample with Si monitor
		34	Earl/COH SiO2 Sidewall Dep, calibrate for 200 nm dep every 2 weeks[c]
	Ellipsometer	35	Measure Si Monitor #1 thickness
	Microscope	36	Inspect
	Solvent bench	37	Sonicate in bath at frequency: 8, intensity: 8, power: low, time~20-30sec
		38	Soak sample in 1165 heated to 80 °C for 10 min, agitate with pipette

		39	Soak sample in 2nd 1165 heated to 80 °C for 5 min, agitate with pipette
		40	2 min Iso, 30 s x 3 rinse & dump DI, N2 dry
	Microscope	41	Inspect, repeat steps 37–40 if necessary
	Dektak	42	Dektak RIDGES pad
n Via Litho	Solvent bench	43	2 min Ace, 2 min Iso, 2 min DI, N2 dry
	PR Bench	44	Dehydration bake on hotplate at ≥110 °C for 2 min, let cool 1 min
		45	Spin LOL 2000, 3 krpm, 10 krpm/s, 30 s (~200 nm thick)
		46	Clean backside of sample with EBR 100
		47	Bake on hotplate at 190 °C for 5 min, let cool for 2 min
		48	Spin SPR220-3.0, 2.5 krpm, 10 krpm/s, 30 s (~2.7 µm thick)
		49	Clean backside of sample with EBR 100
		50	Bake on hotplate at 115 °C for 90 s
	Stepper	51	Load mask #2 n Vias
		52	Load sample onto 2" 500 µm chuck with 180 µm shim, *c*+ pointing up
		53	Run "EX RIDGESTOPN"
		54	Pass: NVIAS
		55	Stepper 2: Expose 0.65s, focus=0, Stepper 1: x sec
	PR Bench	56	Bake on hotplate at 115 °C for 90 s
	Develop bench	57	Develop in 726MIF for 75 s
	Microscope	58	Inspect (verify ~0.5-0.7 µm undercut on LOL 2000), develop more if necessary
	UV Ozone	59	20 min (~6 Å/min)
	Dektak	60	Dektak FACETS pad
n Via Etch	Acid Bench	61	Pour BHF

		62	Etch piece of Si Monitor #1 in BHF (~200 nm/min)
		63	Inspect monitor for hydrophobicity every 10-15s, record total etch time (should take 50 s – 1 min)
		64	Etch sample in BHF for double the monitor etch time
		65	1 min DI, N2 dry
	RIE #5	66	Load bare carrier wafer
		67	O2: 50 sccm, 50 mT, 300 W, 10 min, no He cooling
		68	BCL3/Cl2: 20/5 sccm, 10 mT, 15 W, 3min, no He cooling
		69	Cl2: 10 sccm, 5 mT, 200 W, 2 min, no He cooling
		70	Load sample(s) on carrier wafer (no mounting oil)
		71	BCL3: 10 sccm, 10 mT, 100 W, 2min, no He cooling
		72	Cl2: 10 sccm, 5 mT, 200 W, ~5 min (~120 +/10 nm/min, target n-contact layer), no He cooling
	Solvent bench	73	Strip mask in 1165 heated to 80 °C for 10+ min, agitate with pipette
		74	Move sample to fresh beaker of 1165
		75	Soak sample in 1165 heated to 80 °C for 2 min, agitate with pipette
		76	2 min Iso, 2 min DI, N2 dry
	Microscope	77	Inspect, repeat with 80 °C PRX if necessary
	Dektak	78	Dektak FACETS pad
n Contact Litho	Solvent bench	81	1min Ace, 1min Iso, 1min DI, N2 dry
	PR Bench	82	Dehydration bake on hotplate ≥110 °C ≥2 min, let cool 1 min
		83	Spin HMDS, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)

		84	Spin OCG825, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)
		85	Clean backside of sample with EBR 100
		86	Bake on hotplate at 95 °C for 2 min
	MJB-3 (left aligner only)	87	Load sample onto one of the black chucks
		88	Flood expose 1 s
	PR Bench	89	Let sample outgas for 5 min (VERY IMPORTANT)[g]
		90	Bake on hotplate at 95 °C for 2 min, let cool 1 min
		91	Spin 955CM-1.8, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)
		92	Clean backside of sample with EBR 100
		93	Softbake on hotplate at 95 °C for 90 s
	Stepper	94	Load mask #3 n Contacts
		95	Load sample onto 2" 500 µm chuck with 180 µm shim, *c*+ pointing up
		96	Run "EX RIDGESTOPN"
		97	Pass: NCONTS
		98	no pass shift
		99	Stepper 2: Expose 0.4s, focus=+2, Stepper 1: Expose 2.20 s, focus=0
	Develop bench	100	Develop in 726MIF for 55-60s (~2 µm undercut on OCG825)
		101	30 s x 3 rinse & dump DI, N2 dry
	Microscope	102	Inspect, develop more if necessary
	UV Ozone	103	20 min (~6 Å/min)
	Dektak	104	Dektak CONTACTS pad
N Contact Dep	Acid Bench	105	Etch sample in 1:1 HCL:H2O for 1 min
	E-beam #3	105	Deposit 150/1000/1000/10000 Å Ti/Al/Ni/Au
	Solvent bench	106	Liftoff in 1165 heated to 80 °C for 10+ min, agitate with pipette
		107	Move sample to fresh beaker of 1165

		108	Soak sample in 1165 heated to 80 °C for 2min, agitate with pipette
		109	2 min Iso, 2 min DI, N2 dry
	Microscope	110	Inspect, repeat 1165 if necessary
	Dektak	111	Dektak N-CONTACTS pad
N Contact Anneal	RTA	112	450C 3min N2 5sccm (Sang Ho's recipe- should be optimized)
(optional) ITO Deposition	Acid Bench	113	Etch sample in 1:1 HCL:H2O for 1 min
	E Beam #2 (with heater)	114	Deposit 100 nm ITO with Si monitor Temp: 250C or hotter, 400C max (current heater set to 580C or hotter) O2 flow: ~33sccm (hold at 3e^-4 torr pressure or higher, HV will shut down at 5e^-4torr) Tooling: ~69 for accurate dep rate
	Ellipsometer	115	Measure Si Monitor #2 thickness
(optional) ITO Isolation Etch Litho	Solvent bench	116	1min Ace, 1min Iso, 1min DI, N2 dry
	PR Bench	117	Dehydration bake on hotplate 110C 2min, let cool 1min
		118	Spin HMDS, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20s before spinning)
		119	Spin AZnLOF2020, 3 krpm, 10 krpm/s, 30 s (~2.1 µm thick)
		120	Clean backside of sample with EBR 100
		121	Bake on hotplate at 110 °C for 90 s
	Stepper	122	Load mask #4 - PCONTS
		123	Load sample onto 2" 500 µm chuck with 180 µm shim, *c*+ pointing up
		124	Run "EX RIDGESTOPN"
		125	Pass: ITO
		126	No pass shift stepper 1, check stepper 2
		127	Stepper 1: Expose 0.6 s, focus -6,

	PR Bench	128	Post-exposure bake on hotplate at 110 °C for 60 s
	Develop bench	129	Develop in AZ300MIF for 60 s
		130	30 s x 3 rinse & dump DI, N2 dry
	Microscope	131	Inspect, develop more if necessary
	UV Ozone	132	20 min (~6 Å/min)
	Dektak	133	Dektak CONTACTS pad
(optional) ITO Isolation Etch	RIE #2	134	Vent, use an Iso soaked wipe to clean chamber walls, top plate and platen
		135	Pump down the chamber (DO NOT load samples)
		136	O_2 clean > 30 min: 20 sccm O2, 125 mT, 500 V
		137	MHA coat = 20 min: 4/20/10 sccm M/H/A, 75 mT, 500 V
		138	Vent, load samples
		139	MHA etch = 18 min (17 nm/min, 20% overetch): 4/20/10 sccm M/H/A, 75 mT, 350V
		140	O_2 *in situ* descum = 10 min: 20 sccm O2, 125 mT, 300 V[f]
	Solvent bench	141	Strip PR in 1165 heated to 80 °C for 30+ min, agitate with pipette (it will take a long time to remove negative resist exposed to a dry etch)
		142	Move sample to fresh beaker of 1165
		143	Soak sample in 1165 heated to 80 °C for 2 min, agitate with pipette
		144	2 min Iso, 2 min DI, N2 dry
	Microscope	145	Inspect carefully (PR is difficult to remove), repeat 1165 and use ultrasonics on 'low' if necessary
Contact Pads Litho	Solvent bench	146	1min Ace, 1min Iso, 1min DI, N2 dry
	PR Bench	147	Dehydration bake on hotplate ≥110 °C ≥2 min, let cool 1 min

		148	Spin HMDS, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)
		149	Spin OCG825, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)
		150	Clean backside of sample with EBR 100
		151	Bake on hotplate at 95 °C for 2 min
	MJB-3 (left aligner only)	152	Load sample onto one of the black chucks
		153	Flood expose 1 s
	PR Bench	154	Let sample outgas for 5 min (VERY IMPORTANT)[g]
		155	Bake on hotplate at 95 °C for 2 min, let cool 1 min
		156	Spin 955CM-1.8, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)
		157	Clean backside of sample with EBR 100
		158	Softbake on hotplate at 95 °C for 90 s
	Stepper	159	Load mask #4 - P-contacts (or 5 p-pads)
		160	Load sample onto 2" 500 µm chuck with 180 µm shim, *c*+ pointing up
		161	Run "EX RIDGESTOPN"
		162	Pass: PCONTS
		163	no pass shift
		164	Stepper 2: Expose: 0.4s, focus=+2 Stepper 1: Expose 2.20 s, focus=0
	Develop bench	165	Develop in 726MIF for 60s (~2 µm undercut on OCG825)
		166	30 s x 3 rinse & dump DI, N2 dry
	Microscope	167	Inspect, develop more if necessary
	UV Ozone	168	20 min (~6 Å/min)
	Dektak	169	Dektak CONTACTS pad
	Acid Bench	170	Etch sample in 1:1 HCL:H2O for 1 min (OMIT IF ITO WAS DEPSOITED)

Contact Pads Dep	E-beam #3	170	Deposit 300/10000 Å Pd/Au (150/10000 Å Ti/Au if ITO was used)
	Solvent bench	171	Liftoff in 1165 heated to 80 °C for 10+ min, agitate with pipette
		172	Move sample to fresh beaker of 1165
		173	Soak sample in 1165 heated to 80 °C for 2min, agitate with pipette
		174	2 min Iso, 2 min DI, N2 dry
	Microscope	175	Inspect, repeat 1165 if necessary
	Dektak	176	Dektak CONTACTS pad
Facets Litho	Solvent bench	177	2 min Ace, 2 min Iso, 2 min DI, N2 dry
	PR Bench	178	Dehydration bake on hotplate at ≥110 °C for 2 min, let cool 1 min
		179	Spin LOL 2000, 3 krpm, 10 krpm/s, 30 s (~200 nm thick)
		180	Clean backside of sample with EBR 100
		181	Bake on hotplate at 190 °C for 5 min, let cool for 2 min
		182	Spin SPR220-7.0, 3.5 krpm, 10 krpm/s, 45 s (~6.0 µm thick)
		183	Clean backside of sample with EBR 100 (very important)
		184	Bake on hotplate at 115 °C for 120 s
	Stepper	185	Load mask #5 - Etched Facets
		186	Load sample onto 2" 500 µm chuck with 180 µm shim, *c*+ pointing up
		187	Run "EX RIDGESTOPN"
		188	Pass: DFACE
		189	Stepper 2: Expose 1.35s, focus=0 Stepper 1: Expose: focus=
	PR Bench	189.5	Let sample outgas for 35mins, IMPORTANT
		190	Bake on hotplate at 50C for 60sec, then immediatley move to 115 °C for 90 s

	Develop bench	191	Develop in 726MIF for 105 s
	Microscope	192	Inspect (verify ~0.5-0.7 µm undercut on LOL 2000), develop more if necessary
	UV Ozone	193	20 min (~6 Å/min)
	Dektak	194	Dektak FACETS pad
Facets Etch	Acid Bench	195	Pour BHF
		196	Etch piece of Si Monitor #1 in BHF (~200 nm/min)- or use time from n via cal
		197	Inspect monitor for hydrophobicity every 10-15s, record total etch time (should take 50 s – 1 min)
		198	Etch sample in BHF for double the monitor etch time
		199	1 min DI, N2 dry
	RIE #5	200	Load bare carrier wafer
		201	O2: 50 sccm, 50 mT, 300 W, 10 min, no He cooling
		202	BCL3/Cl2: 20/5 sccm, 10 mT, 15 W, 3min, no He cooling
		203	Cl2: 10 sccm, 5 mT, 200 W, 2 min, no He cooling
		204	Load sample(s) on carrier wafer (no mounting oil)
		205	BCL3: 10 sccm, 10 mT, 100 W, 2min, no He cooling
		206	Cl2: 10 sccm, 5 mT, 200 W, ~30-35 min (~100-150 nm/min), no He cooling
	Solvent bench	207	Strip mask in 1165 heated to 80 °C for 10+ min, agitate with pipette
		208	Move sample to fresh beaker of 1165
		209	Soak sample in 1165 heated to 80 °C for 2 min, agitate with pipette
		210	2 min Iso, 2 min DI, N2 dry
	Microscope	211	Inspect, repeat with 80 °C PRX if necessary

	Dektak	212	Dektak FACETS pad
(optional) Backside N-contact Dep & Liftoff	PR Bench	213	Mount sample upside down on Si wafer with a drop of AZ 4110
		214	Bake on hotplate at 105 °C for >5 min
	E-beam #3	215	Deposit 500/1000/3000 Å Al/Ni/Au
	Solvent bench	216	Soak sample in 1165 heated to 80C until sample detaches from Si wafer[h]
		217	2 min Iso, 2 min DI, N2 dry
	Microscope	218	Inspect, repeat 1165 if necessary
Preliminary testing	Test lab	219	Test devices prior to facet coating (optional)
Clean	Solvent bench	220	3 min Ace, 2 min Iso, 1 min DI, N2 dry (sonicate on high)
	Gasonics	221	Recipe 7, multiple runs if desired[i]
Facet Coating Litho	E-beam #1	222	Blanket deposit 500 Å of Ge with tilt & rotation on, with Si Monitor
	PR Bench	223	Dehydration bake on hotplate 110C 2min, let cool 1min
		224	Spin HMDS, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)
		225	Spin OCG825, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)
		226	Clean backside of sample with EBR 100
		227	Bake on hotplate at 95 °C for 2 min
	MJB-3 (left aligner only)	228	Load sample onto one of the black chucks
		229	Flood expose 1 s
	PR Bench	230	Let sample outgas for 5 min (VERY IMPORTANT)
		231	Bake on hotplate at 95 °C for 2 min, let cool 1 min
		232	Spin 955CM-1.8, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)
		233	Clean backside of sample with EBR 100

		234	Softbake on hotplate at 95 °C for 90 s
	Stepper	235	Load mask # 7 - Facet Coatings
		236	Load sample onto 2" 500 µm chuck with 180 µm shim with *c*+ pointing up
		237	Run "EX RIDGESTOPN"
		238	Pass: DBRS (pass shift = 0)
		239	Stepper 2: Expose: 0.4s, focus=+2 Stepper 1: Expose 2.20 s, focus=0
	Develop bench	240	Develop in 726MIF for 60 s (~2 µm undercut on OCG825)
		241	30 s x 3 rinse & dump DI, N2 dry
	Microscope	242	Inspect, develop more if necessary
Facet Coating	UV Ozone	243	20 min (~6 Å/min)
	Acid Bench	244	Etch piece of Si Monitor in Hydrogen Peroxide to get etch rate
		245	Etch sample for double the monitor etch time (~60 s)
		246	1 min DI, N2 dry
	Veeco IBD	247	Calibrate the IBD for 45 ° platen angle using facet coating calibration
		248	Load samples
		249	Calculate new dep times to account for field vs facet coverage ratio. Use SiO2 time = 1.55*(calibrated SiO2 time), Ta2O5 time = 2.30*(calibrated Ta2O5 time)
		250	Set number of periods (normally 4-7), run recipe
	Solvent bench	251	Liftoff in 1165 heated to 80 °C for 10+ min, agitate with pipette
		252	Move sample to fresh beaker of 1165
		253	Soak sample in 1165 heated to 80 °C for 2 min, agitate with pipette
		254	2 min Iso, 2min DI, N2 dry
	Microscope	255	Inspect, repeat 1165 if necessary

	Acid Bench	256	Etch sample in Hydrogen Peroxide for double the monitor etch time (~60s)
		257	1 m+C155:D260in DI, N2 dry

[a]To reach "boiling" at 80 °C, the hot plate must be set at 120–130 °C.

[b]Either stepper can be used, but the "old" stepper showed better reproducibility and better edge die yield. Plus it is significantly easier to book.

[c]Dep rate increases sharply when a Si target is replaced, then typically decreases slowly over time.

[d]This is the last chance to strip the SiO2 and try again if something looks off. Once you start lift-off there is no going back.

[e]Always heat 1165 in the water bath in bay 7. Glass to hot plate thermal contact is terrible and heating 1165 on a hot plate won't go above about 50 °C. If you heat a sample in a ultrasonics bath someone else may turn it on by accident (this has happened).

[f]The O2 descum removes polymer residue deposited during the MHA etch. Without the descum, the polymer reacts with air and becomes almost impossible to remove (although HF may take it off).

[g]If the sample is not allowed to outgas for a sufficient amount of time before spinning the second layer, bubbles will for in the resist.

[h]If you pry or slide samples off the carrier you may delaminate the Pd/Au pads.

[i]Gasonics hasn't been thoroughly tested to make sure it doesn’t damage the facets, but it shouldn't, and a better facet clean before coatings is needed.

Step	Equipment	#	Process Step	Notes
Surface Clean and Reactivation				
Remove Indium	Acid Bench	1	1:3 HNO_3:HCl (aqua regia) hotplate at 225 °C, 5-10' until soln fades yellow, repeat 2x	Boil HCl, then add HNO_3, then add sample
Tergitol Scrub	Solvent bench	2	Scrub samples in tergitol with swabs to get rid of any residual scum	
Clean	Solvent bench	4	3' Ace, 3' Iso, 2' DI (sonicate on high) N2 dry	
Reactivate	MOCVD lab furnace	5	Reactivate 15' at 600 °C (or use RTA 600C 15 min N2/O2)	
Ridge Formation and SiO2 Deposition				
Ridges Litho	Solvent bench	6	3' Ace, 3' Iso, 2' DI (sonicate on high) N2 dry	
	PR Bench	7	Dehydration bake on hotplate at ≥110 °C for ≥2', cool 1'	
		8	Spin **LOL 2000**, 2 krpm, 10 krpm/s, 30s (~250 nm thick)	mount small samples on blue tape, can spin multiple samples simultaneously
		9	Clean backside with EBR 100	if needed
		10	Bake on center of LH hotplate at **210 °C for 5'**, cool 1'	Actual center T ~194 °C
		11	Spin **955CM-1.8**, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)	
		12	Clean backside with EBR 100	if needed
		13	Soft bake on hotplate **95 °C for 90 s**	
	Stepper #2 (30+')	14	Load mask #1A/B/C/D/E - Ridges	
		15	Load sample onto 2" 500 µm chuck with 130 µm shim with *c*+ pointing up	
		16	"EDIT RIDGESV4B" Check: die size and column number	
		17	"EXEC RIDGESV4B", PASS: "RIDGES"	no pass shift
		18	Expose 0.75 s, focus = -1	
	PR Bench	19	Post-exposure bake on hotplate at **110 °C for 90 s**	
	Develop Bench	20	Develop in **726MIF for 65 s**, DI Rinse, N2 dry	
	Microscope	21	Inspect (0.3-0.5 um undercut on LOL 2000) develop more if necessary	
	UV Ozone	22	1200 s (~6 Å/min)	
Ridges Etch	RIE #5	23	Load bare carrier wafer	

	(2+ hr)	24	Run DAN_01 O2 clean: 20.5 sccm, 10', 5 mTorr, 150 W RF; BCl3/Cl2 pretreat: 20.5 sccm BCl3, 5.2 sccm Cl2, 3', 10 mTorr, 15 W RF; Cl2 etch conditions: 10.2 sccm, 2', 5mTorr, 200 W RF	no He cooling
		25	Repeat DAN_01	
		26	Load sample onto carrier wafer (no mounting oil)	
		27	Run DAN_03, 04 or 05 BCl3 pretreat: 10 sccm, 10', 2', 10 mTorr, 100 W RF; Cl2 Etch: 10 sccm, 5', 5 mTorr, 200 W RF	Dan_03 is 5'
		28	Soak sample in DI water, N2 dry	
	Microscope	29	Inspect	
	Laser Microscope	30	Image RIDGES pad	
	Sputter #3	31	Load silicon calibration piece	
	(3+ hr, start at same time as RIE)	32	Login: Earl Check and run recipe: COH_Ratetestdep for 2100'' (35')	
SiO2 Dep & Liftoff	Ellipsometer	33	Measure SiO2 on Si calibration thickness and index	should be ~ 125 nm (dark blue colored), n=1.47
	Sputter #3	34	Load sample(s) with silicon monitor	
		35	Calculate dep time for 225 nm SiO2. Update and run recipe: COH_SiO2 Sidewall Dep	
	Ellipsometer	36	Measure SiO2 on Si monitor thickness and index	should be ~ 225 nm (gold colored), n=1.47
	Solvent bench	37	Soak sample in 1165 pre-heated to 80 °C for 15'	place sample face-down in beaker
		38	Move sample to 2nd 1165 pre-heated to 80 °C	
		39	Sonicate in bath at frequency: 8, intensity: 8, power: low, time~20-30 s	
		40	swish for 30'' Iso, 30'' DI, N2 dry	
		41	Inspect, repeat steps 37–40 if necessary	
P-Contact Formation				
	Solvent clean	42	2' in each ACE/ISO/DI	
	PR Bench	43	Dehydration bake on hotplate ≥110 °C ≥2', cool 1'	
		44	Spin **HMDS**, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)	
		45	Spin **OCG825**, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)	

Contact Pads Litho		46	Clean backside of sample with EBR 100	if needed
		47	Bake on hotplate at **95 °C for 2'**	
	MJB-3 aligner	48	Load sample onto one of the black chucks	left aligner only
		49	Flood expose 1 s	
	PR Bench	50	Let sample outgas on benchtop for 5' (VERY IMPORTANT)	otherwise, bubbles form in the resist after spinning 2nd layer
		51	Bake on hotplate at **95 °C for 2'**, cool 1'	
		52	Spin **955CM-1.8**, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)	
		53	Clean backside with EBR 100	if needed
		54	Softbake on hotplate at **95 °C for 90 s**	
	Stepper #2 (30+')	55	Load mask: EF V5.gds - Layer 6 Thin Pmetal BackN	for 2-litho p-contact process
		56	Load sample onto 2" 500 µm chuck with 130 µm shim with *c*+ pointing up	
		57	"EDIT RIDGESV4B" Check: die size, column number, right alignment die position	
		58	"EXEC RIDGESV4B", PASS: "PCONTS"	no pass shift
		59	Expose 0.75 s, focus= -1	
	Develop bench	60	Develop in **726MIF for 55-60s** (~2 µm undercut on OCG825), DI Rinse, N2 dry	
	Microscope	61	Inspect, develop more if necessary	
	UV Ozone	62	1200 s (~6 Å/min)	
p-Contact Dep	Acid Bench	63	Mix 1:1 HCl:DI, etch 30 s, DI rinse, N2 dry	removes native oxide, do immediately before contact deposition
	E-Beam #3 (2+ hr)	64	Deposit 300/800 Å Pd/Au narrow metal p-contacts	for adhesion, start dep at 5e-7 torr (use a Ti burn if needed). Pd dep at 0.5 Å/s, ramp to 1 Å/s at 100 Å over 30''
	Solvent bench	65	Place upside-down in 1165 heated to 80 °C for 10+', then liftoff using pipette agitation	for adhesion, do not leave overnight in hot 1165
		66	Move sample to fresh beaker of 1165 and agitate until visibly clean pattern (no Au strands)	
		67	swish for 30'' Iso, 30'' DI, N2 dry	
	Microscope	68	Inspect, repeat steps 65–67 if necessary	
P-Pad Formation				

	Solvent clean	69	2' in each ACE/ISO/DI swishing or sonicating on lowest settings	
	PR Bench	70	Dehydration bake on hotplate ≥110 °C ≥2', cool 1'	
		71	Spin **HMDS**, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)	
		72	Spin **OCG825**, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)	
		73	Clean backside of sample with EBR 100	
		74	Bake on hotplate at **95 °C for 2'**	
	MJB-3 aligner	75	Load sample onto one of the black chucks	left aligner only
		76	Flood expose 1 s	
		77	Let sample outgas for 5' (VERY IMPORTANT)	
	PR Bench	78	Bake on hotplate at **95 °C for 2'** let cool 1'	
		79	Spin **955CM-1.8**, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)	
		80	Clean backside with EBR 100	if needed
		81	Softbake on hotplate at **95 °C for 90 s**	
Contact Pads Litho	Stepper #2 (30+')	82	Load mask #2 - "EF V5.gds- Layer 7: PContPads"	
		83	Load sample onto 2" 500 µm chuck with 130 µm shim with *c*+ pointing up	
		84	"EDIT RIDGESV4B" Check: die size, column number, right alignment die position	
		85	"EXEC RIDGESV4B", PASS: "PCONTS"	no pass shift
		86	Expose 0.75 s, focus= -1	
	Develop bench	87	Develop in **726MIF for 55-60s** (~2 µm undercut on OCG825), DI Rinse, N2 dry	
	Microscope	88	Inspect, develop more if necessary	
	UV Ozone	89	1200 s (~6 Å/min)	
p-Pad Dep	E-Beam #3 (2+ hr)	90	Deposit 300/10,000 Å Ti/Au	
	Solvent bench	91	Place upside-down in 1165 heated to 80 °C for 10+', then liftoff using pipette agitation	do not leave overnight in hot 1165
		92	Move sample to fresh beaker of 1165 and agitate until visibly clean pattern (no Au strands)	
		93	swish for 30'' Iso, 30'' DI, N2 dry	
	Microscope	94	Inspect, repeat steps 91-93 if necessary	
C+ Facet Formation				
	Solvent bench	95	2' in each ACE/ISO/DI swishing	

	PR Bench	96	Dehydration bake on hotplate at ≥110 °C for ≥2', cool 1'	
		97	Spin **HMDS**, 3.5 krpm, 10 krpm/s, 30 s	
		98	Spin **SPR220-7.0**, 3.5 krpm, 10 krpm/s, 45 s (~6 µm thick)	
		99	Clean backside with EBR 100	if needed
		100	Soft bake on hotplate **115 °C for 120 s**	
	Stepper #2 (30+')	101	Load CAIBE mask	
		102	Load sample onto 2" 500 µm chuck with 130 µm shim with ***c+* pointing up**	orientation very important!
		103	"EDIT RIDGESV4B" Check: die size, column number, right alignment die position	
C+ Facets Litho		104	Under CAIBE pass, Y Pass Shift = +0.016 (first etch, shifts pattern DOWN and exposes the c+)	Adjust pass shift if p-pad alignment was off by more than 400 nm in Y. Must align to metal in Y
		105	"EXEC RIDGESV4B", Pass: "CAIBE"	
		106	Expose 1.35 s, focus= -1	
	PR Bench	107	Let sample **outgas for 35'** IMPORTANT	preheat the hotplate at 50 °C
	PR Bench	108	Post-exposure bake on hotplate at **50 °C for 60 s**, then immediately move to **115 °C for 90 s**	
	Develop Bench	109	Develop in **726MIF for 105 s**, DI rinse, N2 dry	
	Microscope	110	Inspect lithography. Check that facets mask aligned in y does not expose any metal. Check that it is the C+ side that is exposed for etching first	
	UV Ozone	111	1200 s (~6 Å/min)	
SiO2 Wet Etch1	Acid Bench	112	Etch piece of Si Monitor #1 in BHF (~200 nm/min)	
		113	Inspect monitor for hydrophobicity every 10-15s, record total etch time (should take 50 s – 1')	
		114	Etch sample in BHF for double the monitor etch time, DI rinse, N2 dry	
C+ Facets Etch	Oxford Ion Mill (2+ hr)	115	Mount samples on chuck with Cu tape such that facets to be etched (c+ side) face LHS	when chuck is mounted into system, it rotates 180°, so the facets will then face the beam
		116	Run: "Speck-Std_Ar_Cl2_norotate_7x" 35', 7x5' etch steps with 6x5' cool steps ;	etch rate 50-60 nm/min

			Gases: Ar 5 sccm to Neutralizer; Ar 10 sccm to Beam; Cl2 20 sccm to Chamber; Beam etch source 200 mA Neutralizer, 200 W RF, 150 mA, 250 Vb, 500 Va; Platen drive "Posn", Platen "Cool" 10 C chiller, Chamber "heat" 40 C	cools substrate and heats chamber walls
	Solvent bench	117	Strip mask in 1165 heated to 80 °C for 10+', agitate with pipette	place sample upside-down in beaker
		118	Move sample to fresh beaker of 1165	
		119	Soak sample in 1165 heated to 80 °C for 2', agitate with pipette	
		120	swish for 30'' Iso, 30'' DI, N2 dry	
	Microscope	121	Inspect that the surface is clean and that the correct side has been etched	
	Laser Microscope	122	Confirm the etch depth and profile	
C- Facet Formation				
	Solvent bench	123	1' Ace, 1' Iso, 1' DI, N2 dry	
	PR Bench	124	Dehydration bake on hotplate at ≥110 °C for ≥2', cool 1'	
		125	Spin **HMDS**, 3.5 krpm, 10 krpm/s, 30 s	
		126	Spin **SPR220-7.0**, 3.5 krpm, 10 krpm/s, 45 s (~6 µm thick)	
		127	Clean backside with EBR 100	if needed
		128	Soft bake on hotplate **115 °C for 120 s**	
C- Facets Litho	Stepper #2 (30+')	129	Load CAIBE mask	
		130	Load sample onto 2" 500 µm chuck with 130 µm shim with ***c*+ pointing up**	orientation very important!
		131	"EDIT RIDGESV4B" Check: die size, column number, right alignment die position	
		132	Under CAIBE pass, Y Pass Shift = -0.016 (2nd etch, shifts pattern DOWN and exposes the c-)	Adjust pass shift if p-pad alignment was off by more than 400 nm in Y. Must align to metal in Y
		133	"EXEC RIDGESV4B", Pass: "CAIBE"	
		134	Expose 1.35 s, focus= -1	
	PR Bench	135	Let sample **outgas for 35'** IMPORTANT	preheat the hotplate at 50 °C
	PR Bench	136	Post-exposure bake at **50 °C for 60 s**, then immediately move to **115 °C for 90 s**	
	Develop Bench	137	Develop in **726MIF for 105 s**, DI rinse, N2 dry	

	Microscope	138	Inspect lithography. Check that facets mask aligned in y does not expose any metal. Check that it is the c- side that is exposed for etching	
	UV Ozone	139	1200 s (~6 Å/min)	
SiO2 Wet Etch2	Acid Bench	140	Etch piece of Si Monitor #2 in BHF (~200 nm/min)	
		141	Inspect monitor for hydrophobicity every 10-15s, record total etch time (should take 50 s – 1')	
		142	Etch sample in BHF for double the monitor etch time, DI rinse, N2 dry	
C- Facets Etch	Oxford Ion Mill	143	Mount samples on chuck with Cu tape such that facets to be etched (c- side) face LHS	(when chuck is mounted into system, it rotates 180°, so the facets will then face the beam)
	(2+ hr)	144	Run: "Speck-Std_Ar_Cl2_norotate_7x"	etch rate 50-60 nm/min
	Solvent bench	145	Strip mask in 1165 heated to 80 °C for 10+', agitate with pipette	place sample upside-down in beaker
		146	Move sample to fresh beaker of 1165	
		147	Soak sample in 1165 heated to 80 °C for 2', agitate with pipette	
		148	swish for 30'' Iso, 30'' DI, N2 dry	
	Microscope	149	Inspect that the surface is clean and that the correct side has been etched	
	Laser Microscope	150	Confirm the etch depth and profile	
N-Contact Formation				
N-contact Dep & Liftoff	PR Bench	151	Mount sample upside down on Si wafer with a drop of AZ 4110	
		152	Bake on hotplate at 105 °C for >5'	
	E-beam #3 (1+ hr)	153	Deposit 500/1000/3000 Å Al/Ni/Au Wait 5' after Ni dep before rotating turret to Au pocket	Al rate < 3 A/s. Ni necessary for heat sink soldering
	Solvent bench	154	Soak sample in 1165 heated to 80 °C until sample detaches from Si wafer	place upside-down in beaker. Do not try to slide or pry samples off
		155	2' Iso, 2' DI, N2 dry	
	Microscope	156	Inspect, repeat 1165 if necessary	
Preliminary Testing	Test lab	157	Test devices prior to facet coating	
HR Back Facet Coating				
	Solvent bench	158	3' Ace, 2' Iso, 1' DI, N2 dry	

	Gasonics	159	Recipe 2, multiple runs if desired	
	E-beam #1	160	Blanket deposit 500 Å of Ge with tilt & rotation on, with Si Monitor	
	PR Bench	161	Dehydration bake on hotplate 110 °C 2', let cool 1'	
		162	Spin **HMDS**, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)	
		163	Spin **OCG825**, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)	
HR Back Facet Coating Litho		164	Clean backside of sample with EBR 100	
		165	Bake on hotplate at **95 °C for 2'**, let cool 1'	
	MJB-3 aligner	166	Load sample onto one of the black chucks	left aligner only
		167	Flood expose 1 s	
	PR Bench	168	Let sample **outgas for 5'** (VERY IMPORTANT)	
		169	Bake on hotplate at **95 °C for 2'**, let cool 1'	
		170	Spin **955CM-1.8**, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)	
		171	Clean backside of sample with EBR 100	
		172	Softbake on hotplate at **95 °C for 90 s**	
	Stepper #2	173	Load mask # 5 - Facet Coatings to coat both facets at once, or mask # 5b HR facet coatings (to coat the back HR mirror only)	
		174	Load sample onto 2" 500 µm chuck with 130 µm shim with *c*+ pointing up	
		175	Run "EX RIDGESV4B"	
		176	Pass: DBRS (pass shift = 0)	
		177	Expose 2.20 s, focus=0	
	Develop bench	178	Develop in **726MIF for 60 s** (~2 µm undercut on OCG825), DI rinse, N2 dry	
	Microscope	179	Inspect, develop more if necessary	
	PE II	180	30 s, 300 mT, 100 W	or UV/ozone 1200''
Ge wet etch	Acid Bench	181	Etch piece of Si Monitor in Hydrogen Peroxide to get etch rate	
		182	Etch sample for double the monitor etch time (~60 s), DI rinse, N2 dry	
IBD cals	Veeco IBD		Nakamura 12, pwd: "nitrides"	
			Calibrate SiO2 dep rate on Si for 1200'' (tilt and rotate throughout), measure n and t in ellipsometry	~0.8 A/s, n=1.47

			Calibrate Ta2O5 dep rate on Si for 1200'', measure n and t in ellipsometry	~1.2 A/s, n=2.27
			Calibrate SiO2-centered fabry-perot (λ/4n Ta2O5, λ/2n SiO2, λ/4n Ta2O5)	"12_LD_SiO2_FP_3PD_45deg"
	Filmetrics		Measure R vs. λ, "notch" is at λ/2n, adjust the SiO2 time for the refined dep rate	Repeat if off by >5nm
	Veeco IBD		Calibrate Ta2O5-centered fabry-perot (λ/4n SiO2, λ/2n Ta2O5, λ/4n SiO2)	"12_LD_Ta2O5_FP_3PD_45deg"
	Filmetrics		Measure R vs. λ and adjust Ta2O5 time	Repeat if off by >5nm
Back Facet Coating			Load samples	
	Veeco IBD		Calculate new dep times to account for field vs facet coverage ratio for 45 ° platen angle: SiO2 time = 1.55*(calibrated SiO2 time); Ta2O5 time = 2.30*(calibrated Ta2O5 time); grid cleans 15' in the beginning and 5' in between steps NOTE: Facet Coatings have had problems 2015-2016, consider process in BETA	HR coatings: start periods with λ/4n SiO2 then λ/4n Ta2O5
			Set number of periods (normally 5–8), run recipe	2 um facet etch depth allows for ~5 period DBR
	Solvent bench		Liftoff in 1165 heated to 80 °C for 10+', agitate with pipette	
			Move sample to fresh beaker of 1165	
			Soak sample in 1165 heated to 80 °C for 2', agitate with pipette	
			2' Iso, 2' DI, N2 dry	
	Microscope		Inspect, repeat 1165 if necessary	
HR or AR Front Facet Coating				
	Solvent bench		1' Ace, 1' Iso, 1' DI, N2 dry	
	PR Bench		Dehydration bake on hotplate ≥110 °C 2', let cool 1'	
			Spin **HMDS**, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)	
			Spin **OCG825**, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)	
			Clean backside of sample with EBR 100	
			Bake on hotplate at **95 °C for 2'**	

	MJB-3 aligner		Load sample onto one of the black chucks	left aligner only
			Flood expose 1 s	
	PR Bench		Let sample **outgas for 5'** (VERY IMPORTANT)	
			Bake on hotplate at **95 °C for 2'**, let cool 1'	
			Spin **955CM-1.8**, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)	
			Clean backside of sample with EBR 100	
			Softbake on hotplate at **95 °C for 90 s**	
Output Facet Coating Litho	Stepper #2		Load mask # 5c - Front facet coatings (if used #5b above)	
			Load sample onto 2" 500 µm chuck with 130 µm shim with *c*+ pointing up	
			Run "EX RIDGESV4B"	
			Pass: DBRs	
			Expose 2.20 s, focus = 0	
	Develop bench		Develop in **726MIF for 60 s** (~2 µm undercut on OCG825), DI rinse, N2 dry	
	Microscope		Inspect, develop more if necessary	
	PEII		30 s, 300 mT, 100 W	
	Acid Bench		Etch piece of Si Monitor in Hydrogen Peroxide to get etch rate	
			Etch sample for double the monitor etch time (~60 s), DI rinse, N2 dry	
Front Facet Coating	Veeco IBD		Re-calibrate IBD if it has been more than 2 days since the HR facet coating	
			Load samples	
			Calculate new dep times: SiO2 time = (1.59*calibrated SiO2 time), Ta2O5 time = 2.50*(calibrated Ta2O5 time)	
			Set number of periods (normally 2 – 3 for HR/HR coating or single SiO2 for AR coating), run recipe	AR coatings: SiO2 single layer
	Solvent bench		Liftoff in 1165 heated to 80 °C for 10+', agitate with pipette	
			Move sample to fresh beaker of 1165	
			Soak sample in 1165 heated to 80 °C for 2', agitate with pipette	
			2' Iso, 2' DI, N2 dry	
	Microscope		Inspect, repeat 1165 if necessary	
Cu Heat Sink Mounting				

	Packaging Lab Dissecting Microscope		Materials: heater and probe mount, wide Cu stub mount, screw for stub, Pb Sn Ag solder foils, superior flux #3-(glutamic acid, HCl), optical table screws, razor blade, Q-tips	for cw testing. Parts in drawer to right of microscope
			file Cu stub to size of substrate with 400 grit sandpaper	
			screw down heater and probe setup to scope stage	
			screw stub to heater	
Heat Sink Mounting			place sized solder foil on stub and press foot pedal to start heater and melt foil, use some flux to help	takes ~90 s to heat up
			scrape solder and reflow until it stops migrating	remove foot from pedal because takes a while to cool
			let cool, add some more flux, then add sample	
			use probe mount to push down on the LD sample in the center of pattern to hold it in place	
			heat until reflow and wets, let cool	

Appendix B: SiLENSe Parameters

The following is taken from STR Group's website:

http://www.str-soft.com/learn/InAlGaN_Alloys/index.htm

Table 1 Lattice constants of binary nitrides at 300 K.

Ref.	*a*(nm)			*c*(nm)		
	AlN	GaN	InN	AlN	GaN	InN
[1]	0.3111	0.3182	0.3540	0.4980	0.5185	0.5705
[2]	0.3112	0.3189	0.3540	0.4982	0.5185	0.5705
[3]		0.3188			0.5186	
[4]	0.3091	0.3160	0.3528	0.4952	0.5138	0.5684

Table 2 Stiffness constants of binary nitrides at 300 K(GPa).

C_{ij} (GPa)	Ref.	AlN		GaN		InN	
		exp.	calc.	exp.	calc.	exp.	calc.
C_{11}	[2]	345	396	374	367	190	223
	[4]	345, 411	398	391	396		271
	[5]	345, 411	398	365, 377, 390	350		
C_{12}	[2]	125	137	106	135	104	115
	[4]	125, 149	140	143	144		124
	[5]	125, 149	142	135, 160, 135	140		
C_{13}	[2]	120	108	70	103	121	92
	[1]	120		114		94	
	[4]	120, 99	127	108	100		94

	[5]	120, 99	112	114, 106	104		
C_{33}	[2]	395	373	379	405	182	224
	[1]	395		381		200	
	[4]	395, 389	382	399	392		200
	[5]	395, 389	383	381, 398	376		
C_{44}	[2]	118	116	101	95	10	48
	[4]	118, 125	96	103	91		46
	[5]	118, 125	127	109, 81, 105	101		

Table 3 Most reliable stiffness constants of binary nitrides at 300 K (GPa).

	AlN	GaN	InN
C_{11} (GPa)	395	375	225
C_{12} (GPa)	140	140	110
C_{13} (GPa)	115	105	95
C_{33} (GPa)	385	395	200
C_{44} (GPa)	120	100	45
v=C13/(C13+C33)	0.23	0.21	0.32

Table 4 Data on the piezoelectric tensor of binary nitrides (C/m2) [6].

	e_{33}	e_{31}	e_{15}	e_{14}
GaN (electromechanical coefficients)	1.0	-0.36	-0.3	
GaN (mobility)	0.44	-0.22	-0.22	0.375
GaN (from optical phonons)	0.65	-0.33	-0.33	0.56
GaN (ab initio)	0.73	-0.49		
InN (from optical phonons)	0.43	-0.22	-0.22	0.37
InN (ab initio)	0.97	-0.57		

AlN (surface acoustic waves)	1.55	-0.58	-0.48	
AlN (ab initio)	1.46	-0.60		

Table 5 Polarization parameters and dielectric constants of binary nitrides.

	AlN	GaN	InN
Spontaneous polarization P_z^s (C/m2)	-0.081	-0.029	-0.032
Piezoelectric tensor e_{33} (C/m2)	1.55	0.65	0.43
Piezoelectric tensor e_{31} (C/m2)	-0.58	-0.33	-0.22
Piezoelectric tensor e_{15} (C/m2)	-0.48	-0.33	-0.22
Dielectric constant ε_{33}	8.5	8.9	15.3

Table 6 Band structure and deformation potential parameters of binary nitrides.

	AlN	GaN	InN
Bandgap E_G at T=0 (eV)	6.25	3.51	0.69
Varshni parameter a (meV/K)	1.799	0.909	0.404
Varshni parameter b (K)	1462	830	454
Crystal field splitting (eV)	-93.2	22.3	37.3
Spin-orbital splitting (eV)	11.1	11.1	11.1
InGaN bowing parameter (eV)	1.2		
AlGaN bowing parameter (eV)	1.0		
AlInN bowing parameter (eV)	4.5		

Table 7 Effective masses of electrons and holes in binary nitrides at 300 K.

	AlN	GaN	InN

	⊥	||	⊥	||	⊥	||
m_n	0.25	0.25	0.2	0.2	0.1	0.1
m_{lh}	1.95	0.25	1.1	0.15	1.35	0.1
m_{hh}	1.95	2.58	1.1	1.65	1.35	1.45
m_{so}	0.23	1.93	0.15	1.1	0.09	1.54

Table 8 Optical parameters of binary nitrides at 300 K.

Material		E_0 (eV)	A_1	Γ_1 (eV)	E_1 (eV)	ε_∞	A_0	Γ_0 (eV)
AlN	ordinary	6.05	1.4	0.8	8.05	2.8	2.6	0.55
	extraordinary		1.6					
InN	ordinary	0.7	1.6	1.2	5.39	5.7	2.5	0.85
	extraordinary		2.0	0.85		5.6	3.3	1.35
GaN	ordinary	3.6	1.1	0.9	7	4.1	1.2	1.1
	extraordinary		1.25					